

1	Cover Sheet
2	System Block Diagram
3	Intel LGA775 CPU - Signals
4	Intel LGA775 CPU - Power
5	Intel LGA775 CPU - GND
6	nVidia C55 - CPU / PCI-E
7	nVidia C55 - HT Link / Power
8	nVidia C55 - Memory A0
9	nVidia C55 - Memory A1
10	nVidia C55 - Gnd
11	DDR II DIMM 1 & 2
12	DDR II DIMM 3 & 4
13	DDR II Termination / EMI
14	nVidia BR04 - C55 Side
15	nVidia BR04 - PCIE x16 Slot
16	nVidia BR04 - Power / Gnd
17	nVidia MCP55 - HT / PCI / LPC
18	nVidia MCP55 - PCI-E
19	nVidia MCP55 - SATA / IDE / RGMII
20	nVidia MCP55 - Audio / USB / GPIO
21	nVidia MCP55 - PWR & GND
22	NB PCI-E x16 Pri / Sec Slot
23	SB PCI-E x16 Pri / Sec Slot
24	SB PCI-E x1 / PCI Slot
25	Gigabit PHY 0 - RTL8211BL
26	Gigabit PHY 1 - RTL8211BL
27	1394 Controller - JMB381
28	JMicron JMB363
29	Super I/O - F71882FG
30	Fan Controller
31	uPI ACPI Solution
32	uPI Power Regulator
33	VRD11- ISL6322 4 Phase 2 Channel
34	Front / Rear USB Connectors
35	ATX / Front Panel / LED
36	Manual Parts
37	Power On/Off Sequence
38	System Reset Map
39	Syatem Power Map
40	GPIO & Jumper Setting
41	Project History

MS-7510

Version : 1.1 *Diamond Edition*

CPU :

Intel Wolfield Family and Yorkfield Family Processor
Intel Conroe Family and Kentsfield Family Processor
Intel Pentium D Processor 900 and 800 Sequence
Intel Pentium 4 Processor 600 and 500 Sequence

System Chipset :

nVidia C72XE [C55 + BR04]
nVidia MCP55P

On Board Chipset :

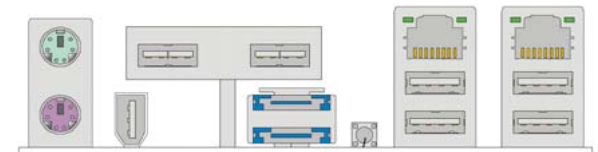
Azalia Codec -- RealTek ALC888
GB PHY 1 -- RealTek RTL8211BL
GB PHY 2 -- RealTek RTL8211BL
VRM 11 -- Intersil ISL6322
ACPI Controller -- uPI Solution
IEEE 1394a Controller -- JMicron JMB381
eSATA Controller -- JMicron JMB363
Super I/O -- FinTek F71882FG
SPI Flash 8Mb

Main Memory :

2 Channel DDR II * 4 (Max 8GB)

Expansion Slot :

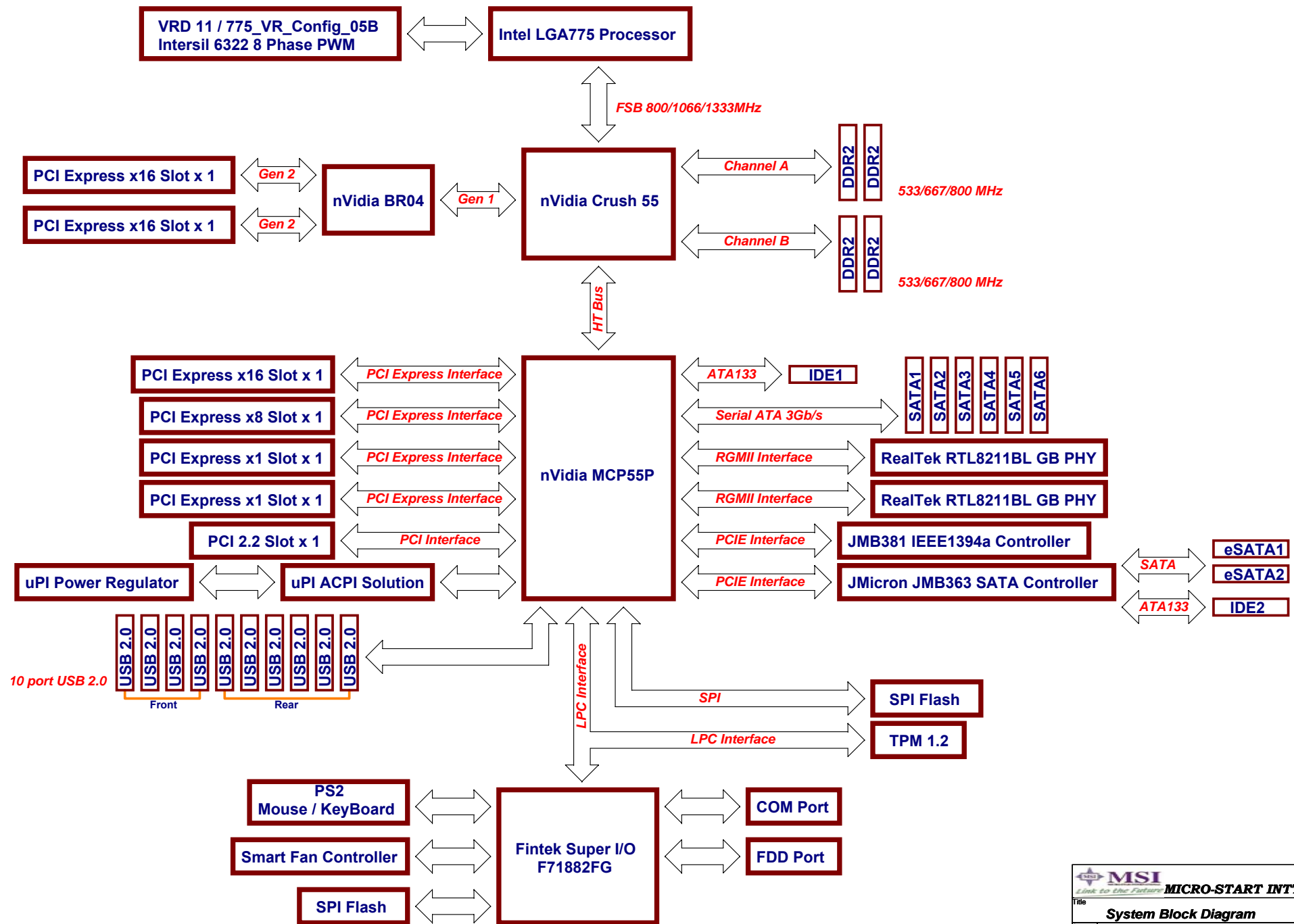
PCI Express x16 Slot * 3
PCI Express x8 Slot * 1
PCI Express x1 Slot * 2
PCI Slot * 1



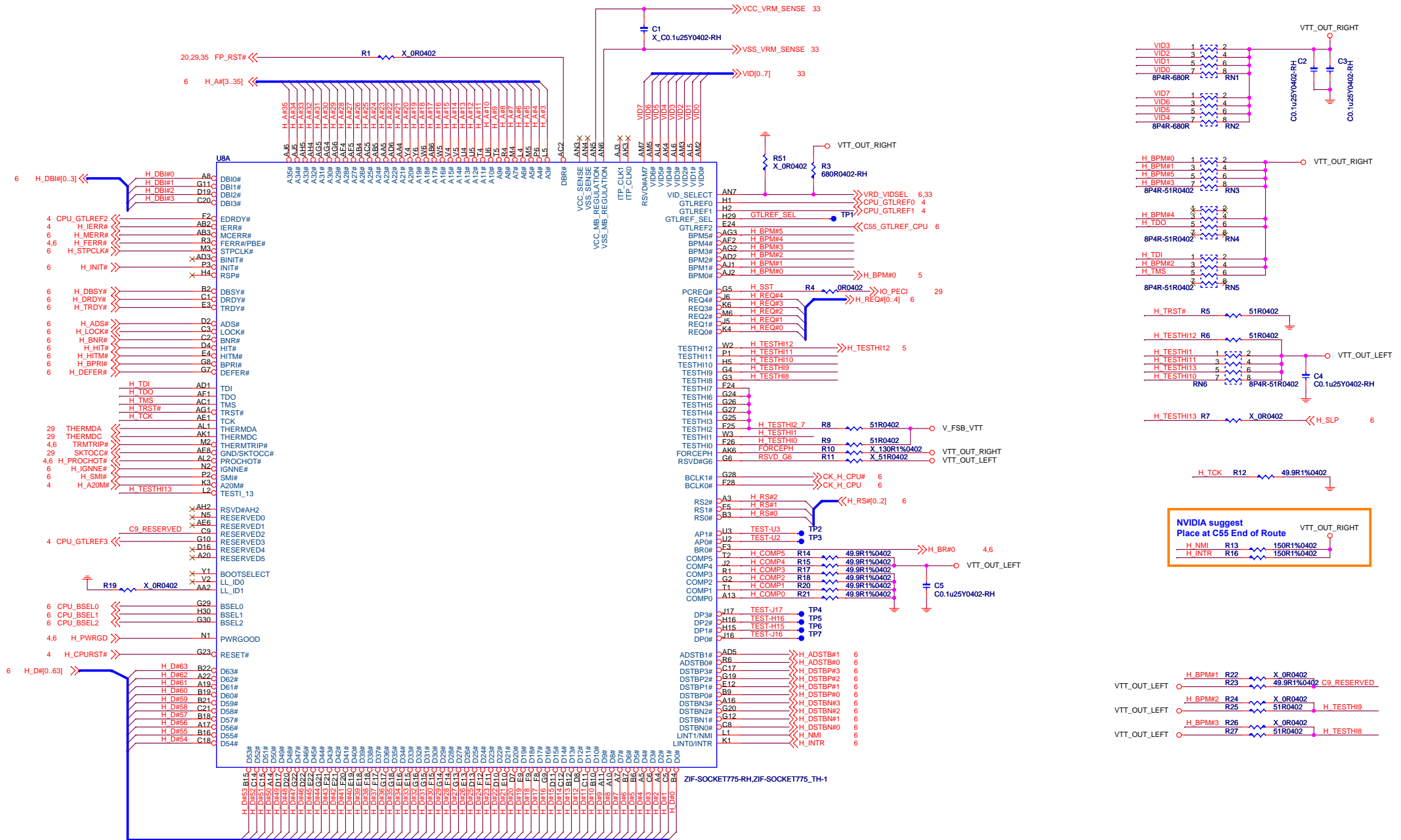
ERP No.	Config Item	PlatForm or Option	Option Select
7510-010	Cfg-CRV	C55 + BR04 + MCP55P + RTL8211BL + JMB381 + JMB363 + F71882FG + MS-4132 + PCB 1.0	STD
7510-02S	Cfg-STD	C55 + BR04 + MCP55P + RTL8211BL + JMB381 + JMB363 + F71882FG + MS-4132 + PCB 1.1	STD

MICRO-STAR INT'L CO.,LTD.		
Title Cover Sheet		
Size	Document Number MS-7510	Rev 1.1
Date: Tuesday, January 22, 2008	Sheet 1	of 41

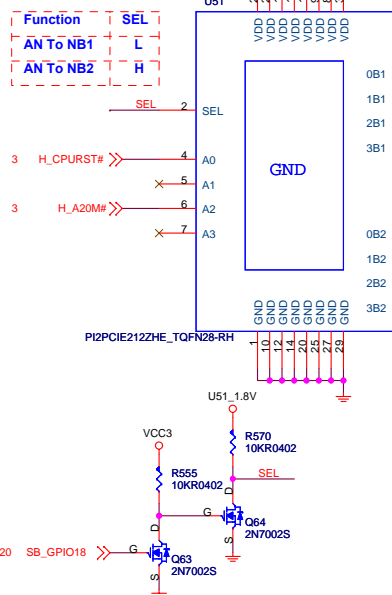
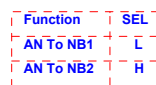
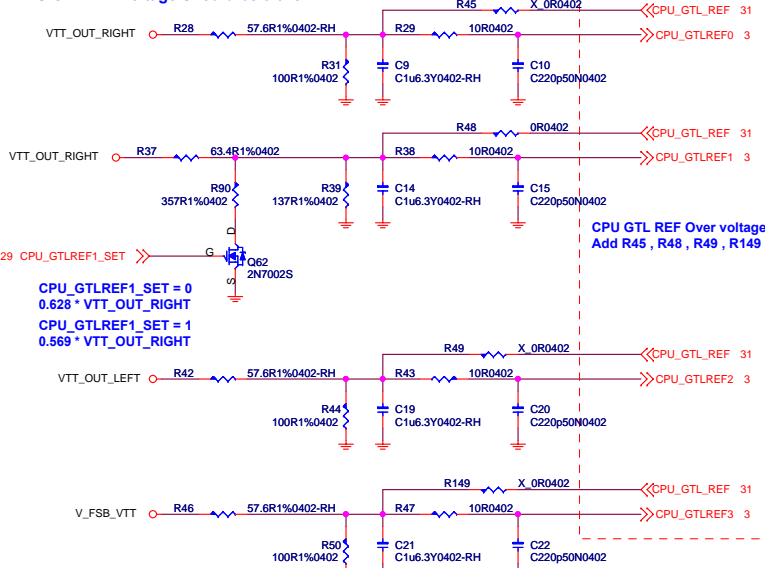
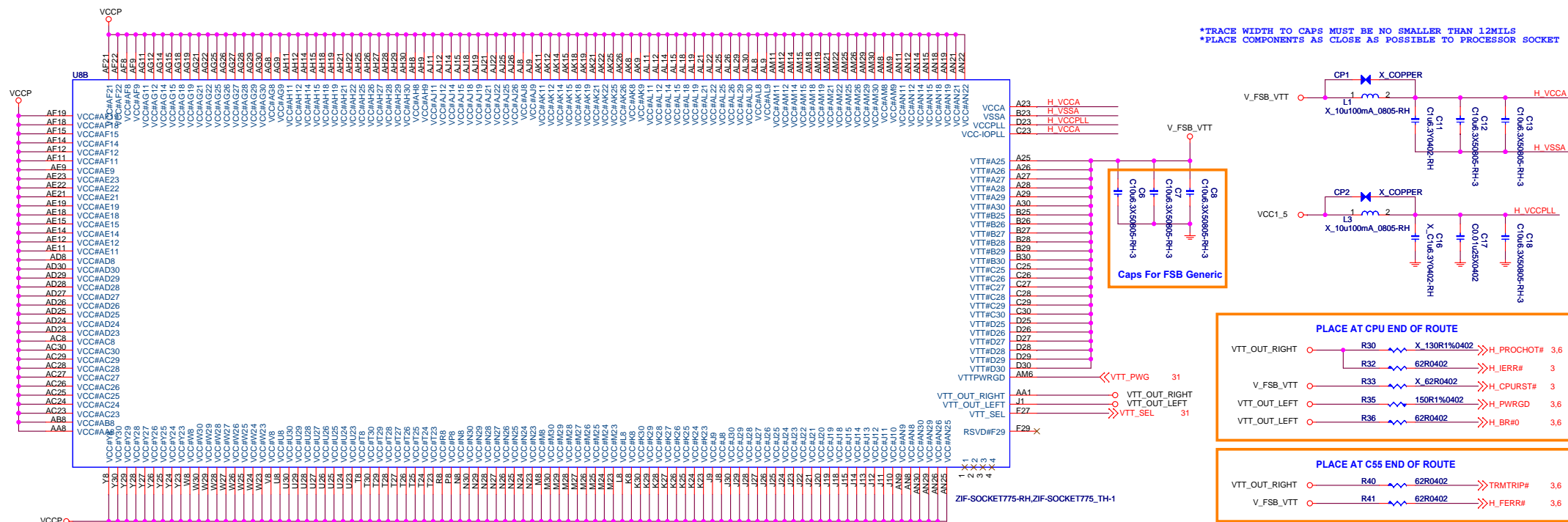
System Block Diagram



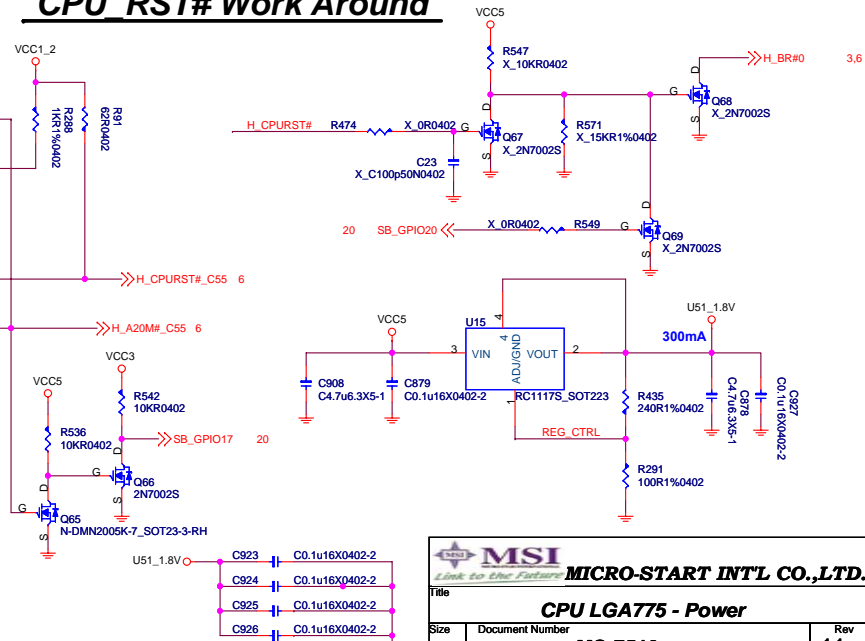
CPU LGA775 - Signals



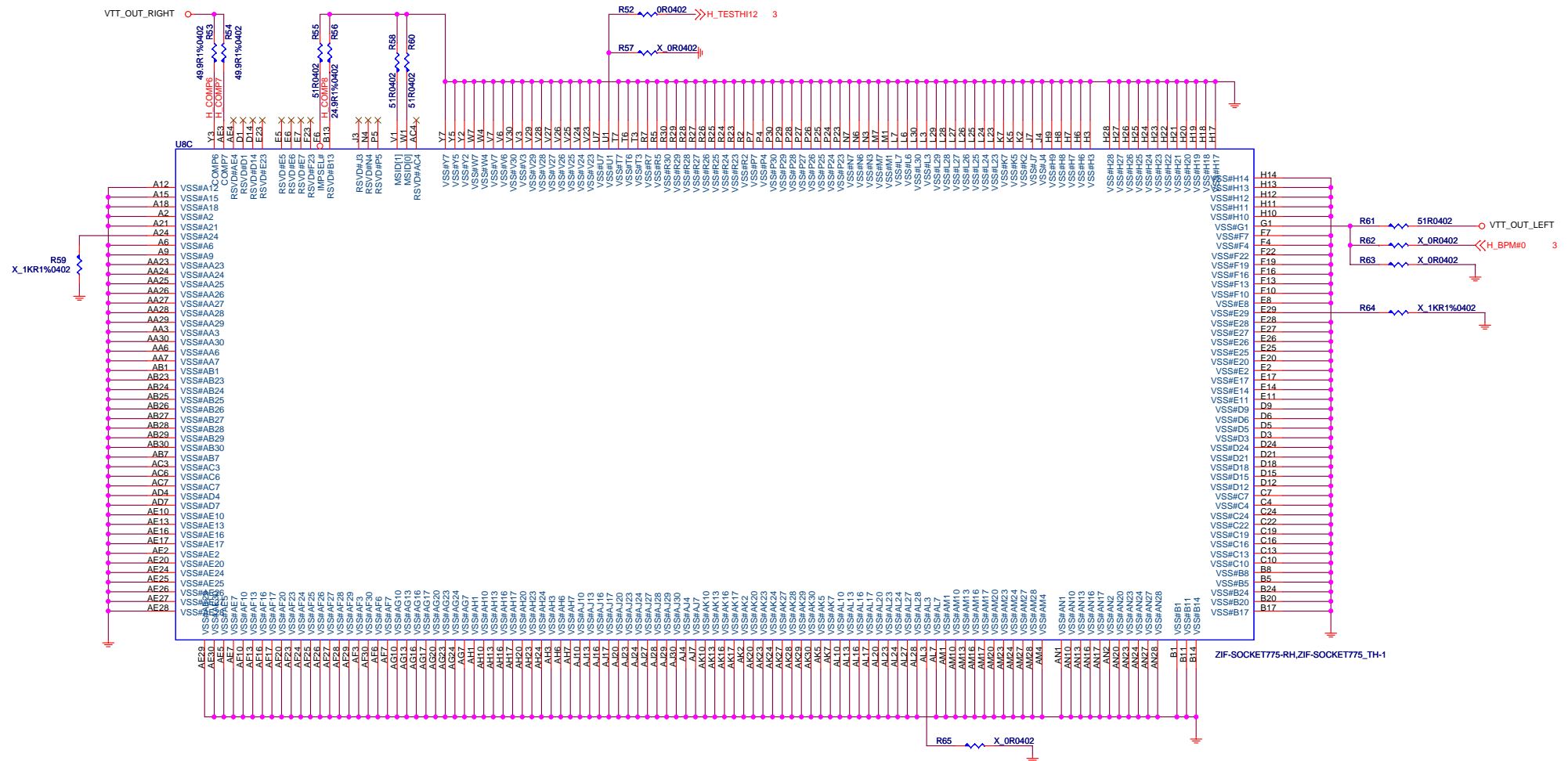
CPU LGA775 - Power



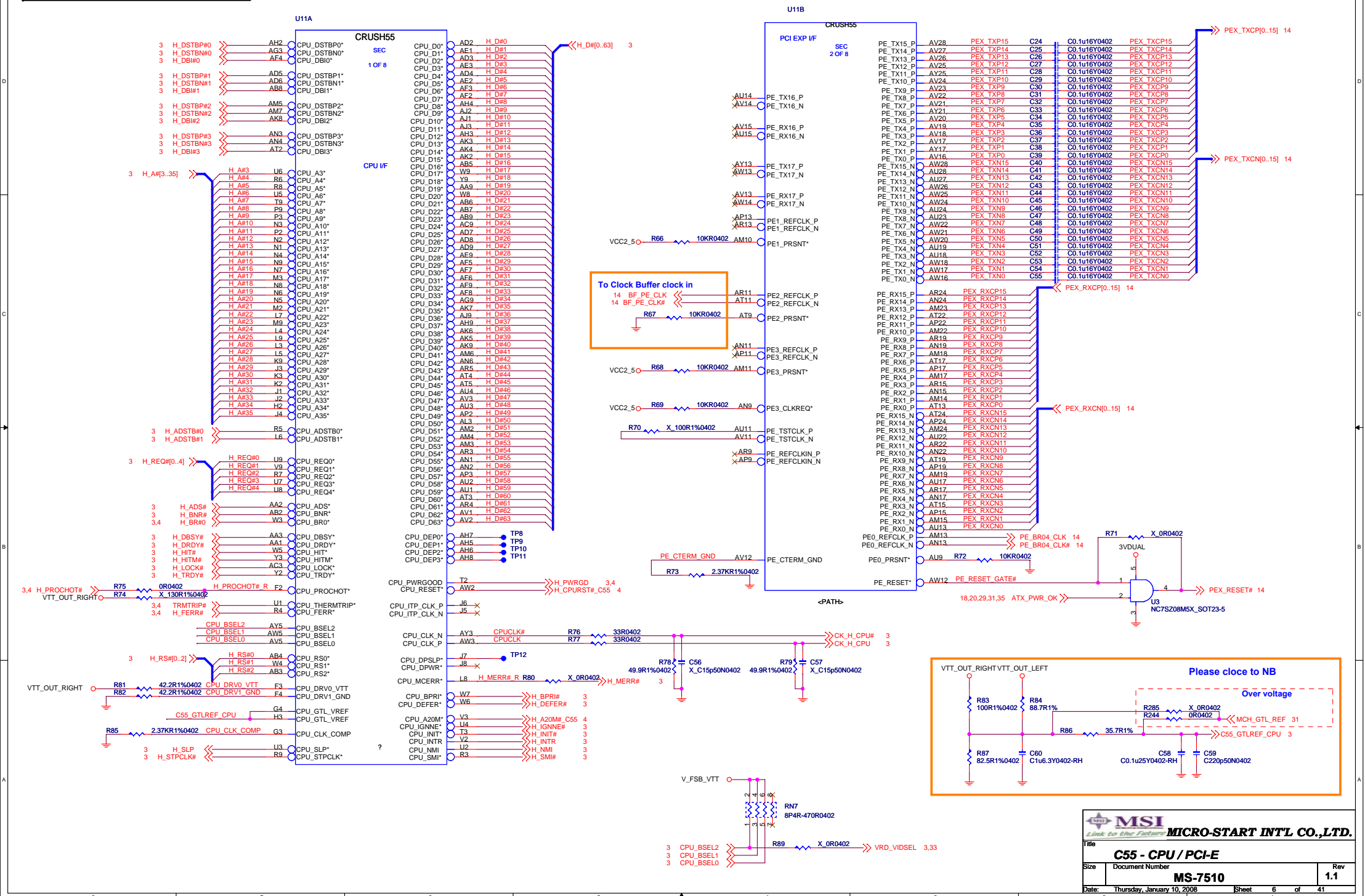
CPU_RST# Work Around



CPU LGA775 - Gnd



C55 - CPU / PCI-E

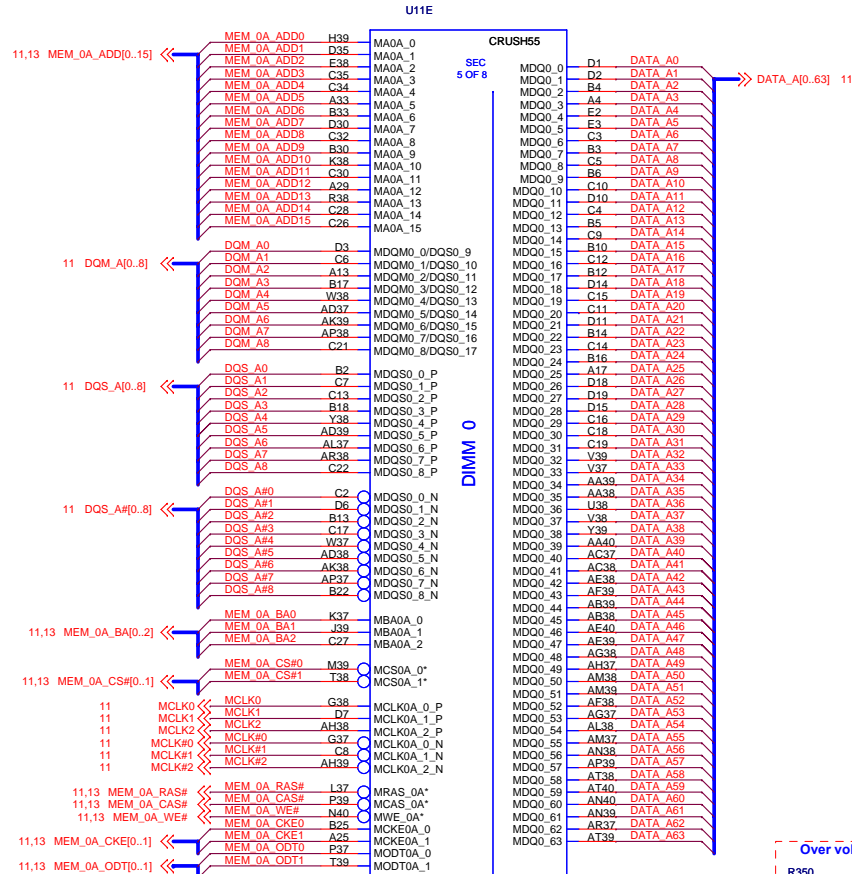


C55 - HT Link / Power

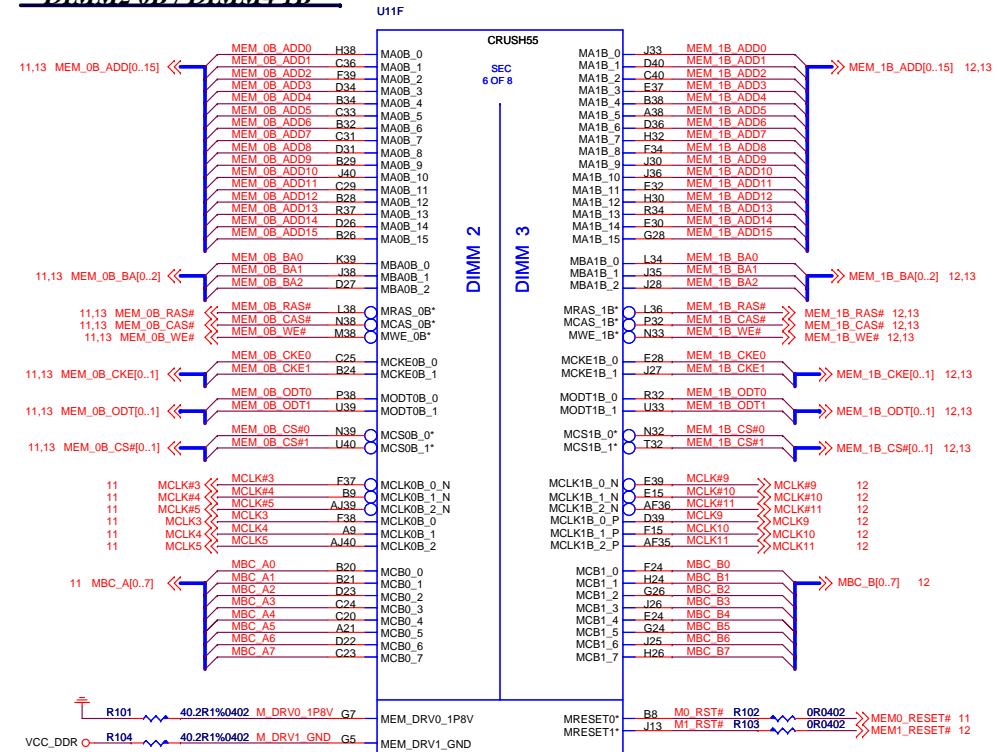
File: **C55 - HT Link / Power**
 Size: **MS-7510**
 Document Number: **MS-7510**
 Date: **Thursday, January 10, 2008**
 Sheet: **7** of **41**
 Rev: **1.1**

C55 - Memory A0

DIMM1 0A



DIMM2 0B / DIMM4 1B



DATA 0	DIMM 1	ADDR 0A / CNTL 0A
	DIMM 2	ADDR 0B / CNTL 0B
DATA 1	DIMM 3	ADDR 1A / CNTL 1A
	DIMM 4	ADDR 1B / CNTL 1B

DIMM3 1A

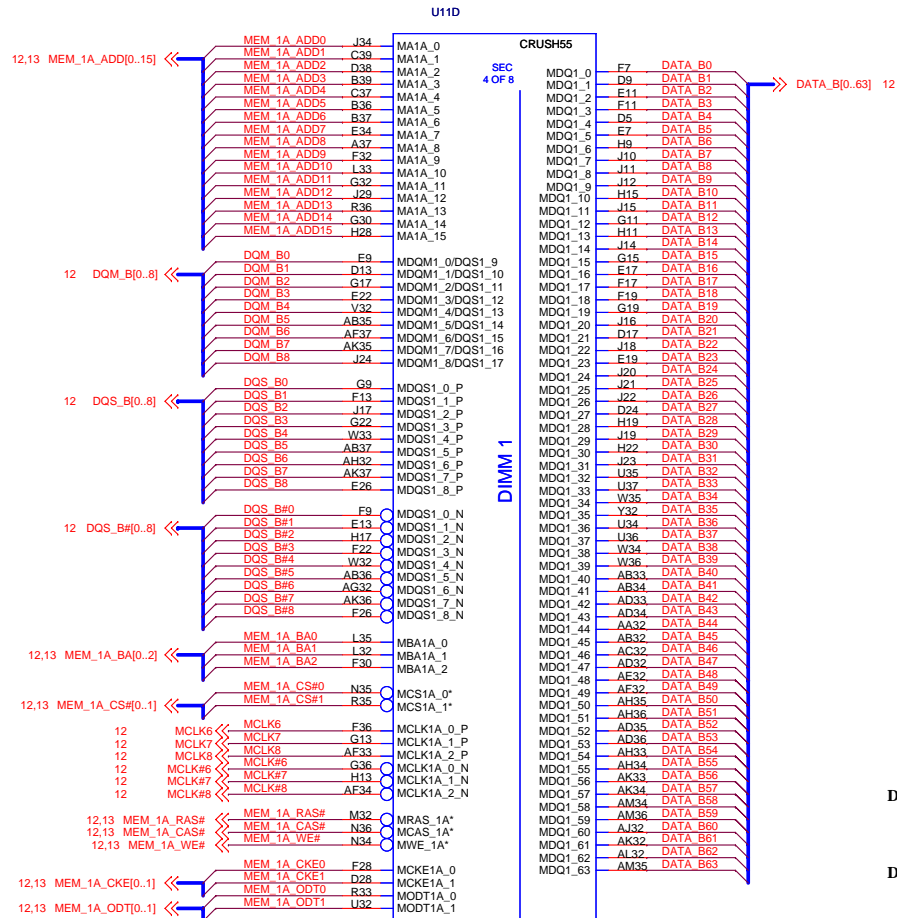


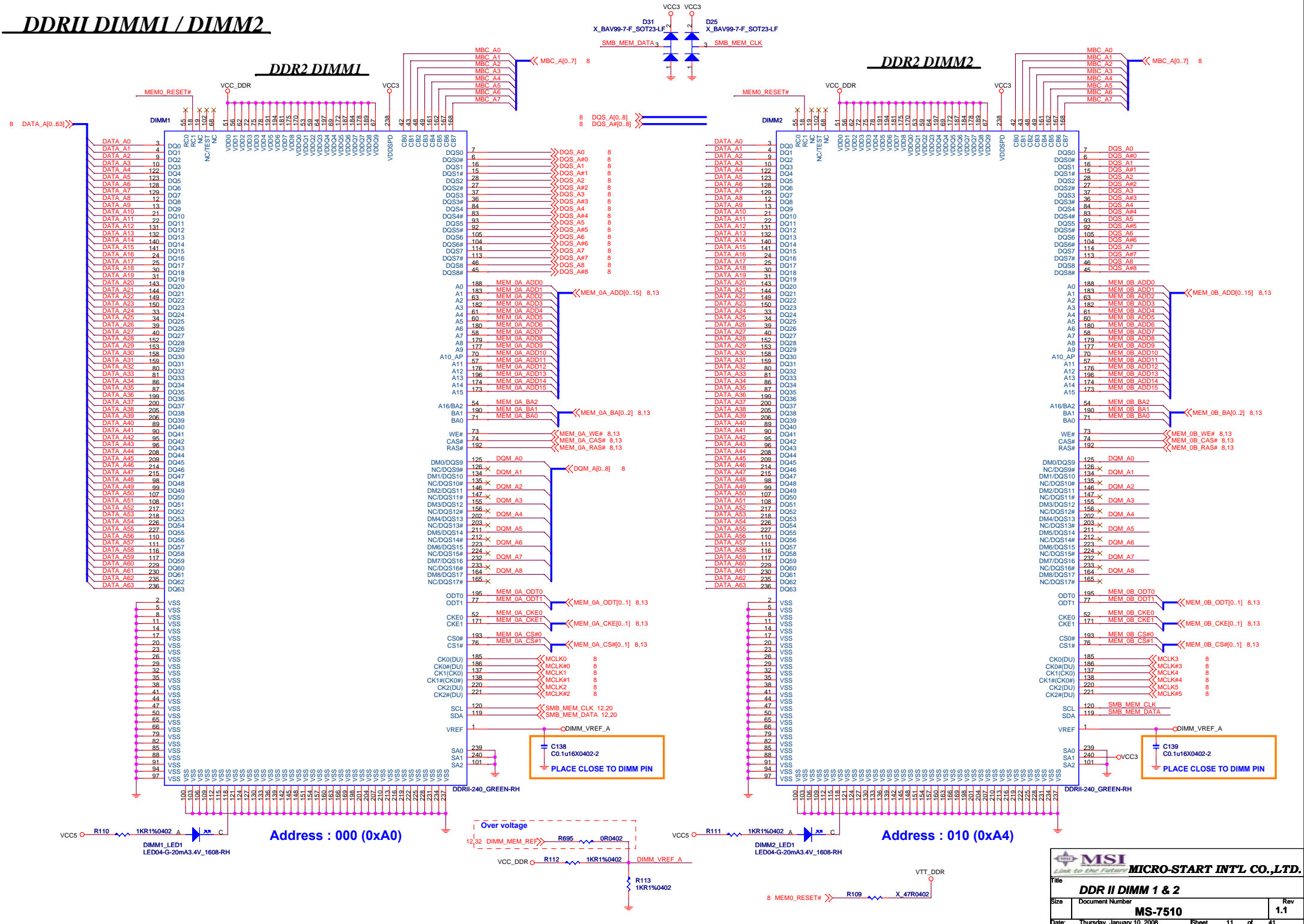
Diagram illustrating the 8-bit data bus connections for DIMM 1 and DIMM 2:

- DATA 0** is connected to **DIMM 1** (ADDR 0A / CNTL 0A) and **DIMM 2** (ADDR 0B / CNTL 0B).
- DATA 1** is connected to **DIMM 3** (ADDR 1A / CNTL 1A) and **DIMM 4** (ADDR 1B / CNTL 1B).

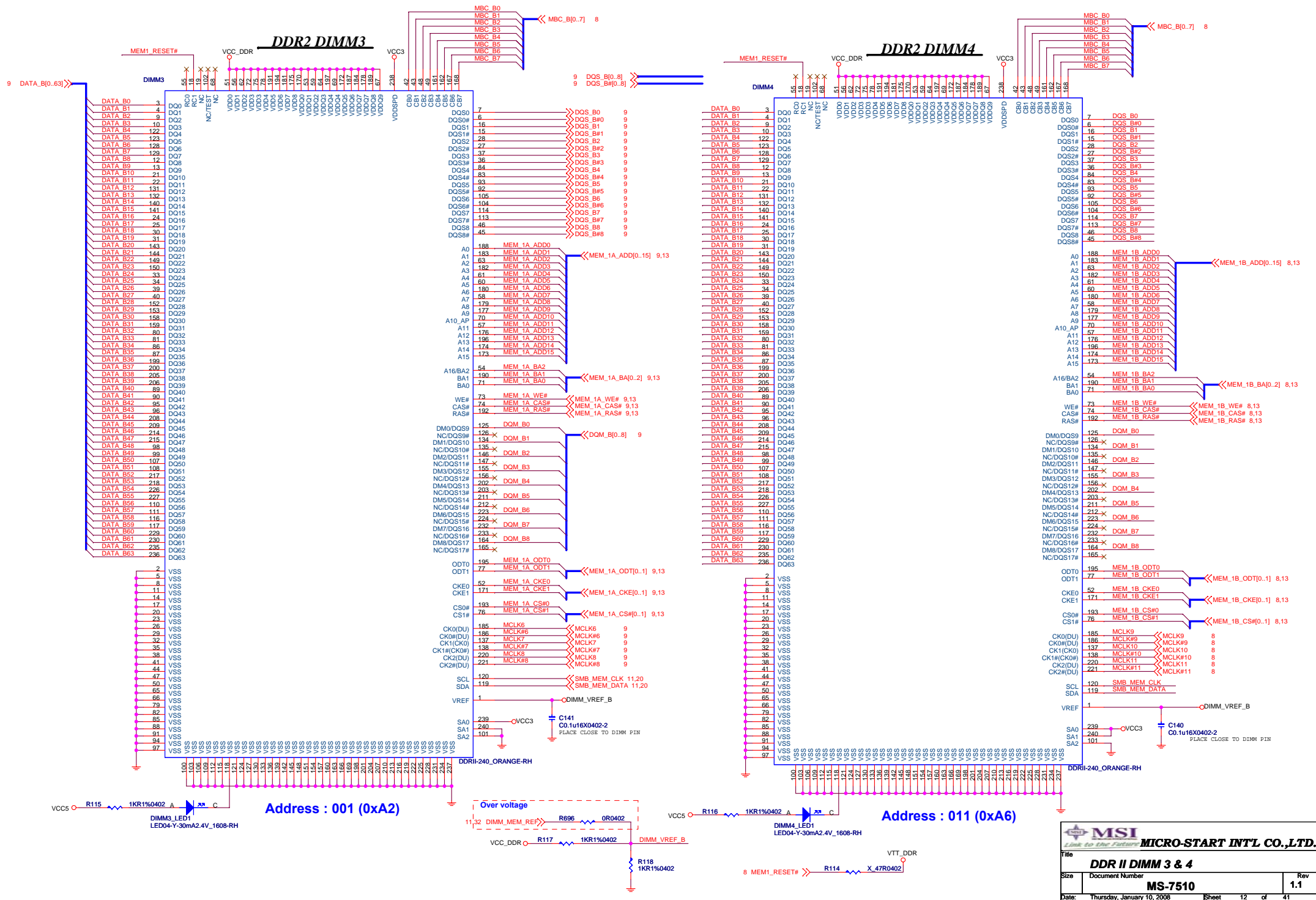
C55 - Gnd



DDR4 DIMM1 / DIMM2



DDRII DIMM3 / DIMM4



Channel A

VTT_DDR

C142 C0.1u16X0402-2

C144 C0.1u16X0402-2

C146 C0.1u16X0402-2

C148 C0.1u16X0402-2

C150 C0.1u16X0402-2

C152 C0.1u16X0402-2

C154 C0.1u16X0402-2

C156 C0.1u16X0402-2

C158 C0.1u16X0402-2

C160 C0.1u16X0402-2

C162 C0.1u16X0402-2

C164 C0.1u16X0402-2

C166 C0.1u16X0402-2

C168 C0.1u16X0402-2

C170 C0.1u16X0402-2

C172 C0.1u16X0402-2

C174 C0.1u16X0402-2

Channel B

VTT_DDR

C143 C0.1u16X0402-2

C145 C0.1u16X0402-2

C147 C0.1u16X0402-2

C149 C0.1u16X0402-2

C151 C0.1u16X0402-2

C153 C0.1u16X0402-2

C155 C0.1u16X0402-2

C157 C0.1u16X0402-2

C159 C0.1u16X0402-2

C161 C0.1u16X0402-2

C163 C0.1u16X0402-2

C165 C0.1u16X0402-2

C167 C0.1u16X0402-2

C169 C0.1u16X0402-2

C171 C0.1u16X0402-2

C173 C0.1u16X0402-2

C175 C0.1u16X0402-2

VTT_DDR				VTT_DDR			
MEM OA ADD10	1	2		MEM OA ADD10	1	2	
MEM OA BA0	3	4		MEM OA BA1	3	4	
MEM OB BA0	5	6		MEM OB ADD10	5	6	
MEM OB BA1	7	8		MEM OB ADD11	7	8	
8P4R-47R0402			RN9	8P4R-47R0402			RN10
MEM OA ADD3	1	2		MEM OA ADD6	1	2	
MEM OB ADD2	3	4		MEM OB ADD3	3	4	
MEM OB ADD4	5	6		MEM OB ADD1	5	6	
MEM OA ADD2	7	8		MEM OA ADD4	7	8	
8P4R-47R0402			RN13	8P4R-47R0402			RN14
MEM OB ADD8	1	2		MEM OB ADD9	1	2	
MEM OB ADD6	3	4		MEM OB ADD7	3	4	
MEM OB ADD5	5	6		MEM OA ADD8	5	6	
MEM OB ADD4	7	8		MEM OA ADD5	7	8	
8P4R-47R0402			RN19	8P4R-47R0402			RN20
MEM OA ADD12	1	2		MEM OB ADD14	1	2	
MEM OA ADD11	3	4		MEM OB ADD15	3	4	
MEM OB ADD11	5	6		MEM OA ADD12	5	6	
MEM OA ADD7	7	8		MEM OA ADD9	7	8	
8P4R-47R0402			RN21	8P4R-47R0402			RN22
MEM OB CS#0	1	2		MEM OA RAS#	1	2	
MEM OB CAS#	3	4		MEM OA CS#0	3	4	
MEM OA WE#	5	6		MEM OB RAS#	5	6	
MEM OA CAS#	7	8		MEM OB WE#	7	8	
8P4R-47R0402			RN25	8P4R-47R0402			RN27
MEM OA BA2	1	2		MEM OA CKE1	1	2	
MEM OB BA2	3	4		MEM OA CKE0	3	4	
MEM OB BA2	5	6		MEM OB CKE0	5	6	
MEM OA ADD14	7	8		MEM OA ADD15	7	8	
8P4R-47R0402			RN29	8P4R-47R0402			RN30
MEM OB ODT1	1	2		MEM OB ODT0	1	2	
MEM OA ADD13	3	4		MEM OA ODT0	3	4	
MEM OA CS#1	5	6		MEM OB CS#1	5	6	
MEM OA ODT1	7	8		MEM OB ADD13	7	8	
8P4R-47R0402			RN36	8P4R-47R0402			RN33

[illegible]

VCC_DDR

C176 || X_C10u10Y0805

C178 || X_C10u10Y0805

C180 || X_C10u6.3X50805-RH-3

C182 || X_C10u6.3X50805-RH-3

C184 || X_C10u6.3X50805-RH-3

C186 || X_C10u6.3X50805-RH-3

VCC_DDR

C177 || C0.1u16X0402-2

C179 || C0.1u16X0402-2

C181 || C0.1u16X0402-2

C183 || C0.1u16X0402-2

C185 || C0.1u16X0402-2

C187 || C0.1u16X0402-2

C188 || C0.1u16X0402-2

C189 || C0.1u16X0402-2

C190 || C0.1u16X0402-2

C191 || C0.1u16X0402-2

C192 || C0.1u16X0402-2

C193 || C0.1u16X0402-2

C194 || C0.1u16X0402-2

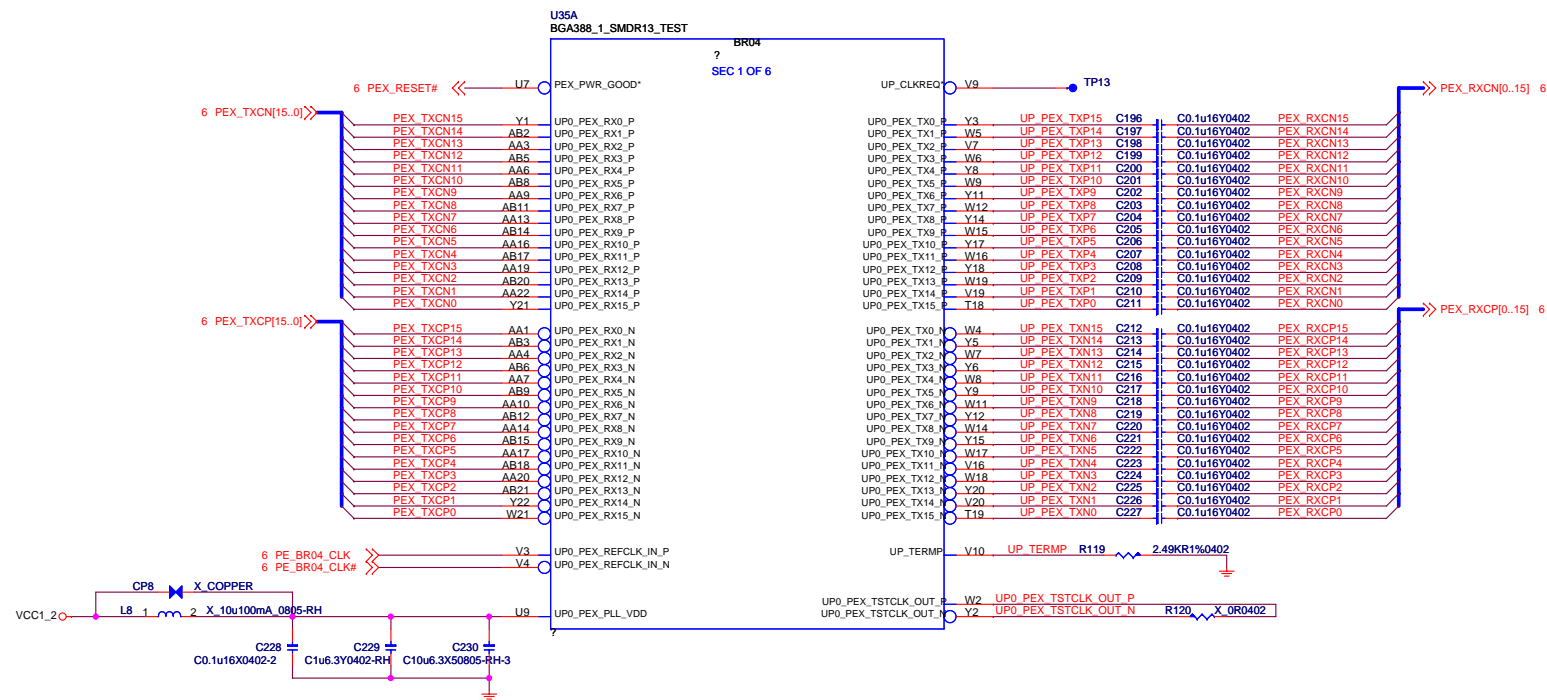
C195 || C0.1u16X0402-2

The schematic diagram illustrates the PCB layout for the system, organized into several functional blocks:

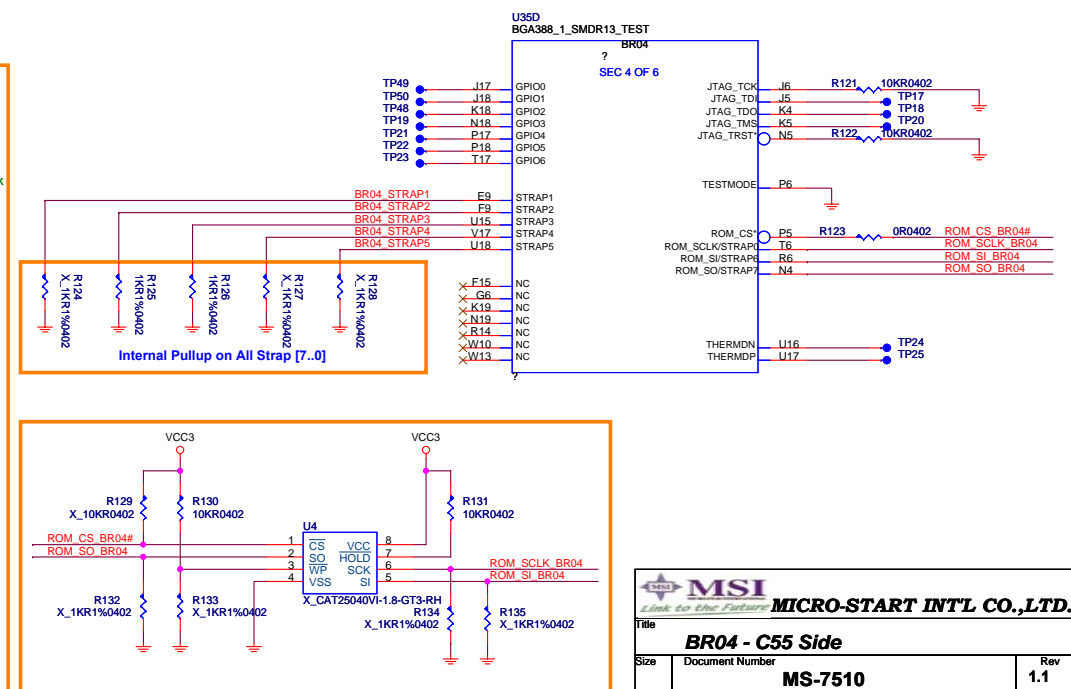
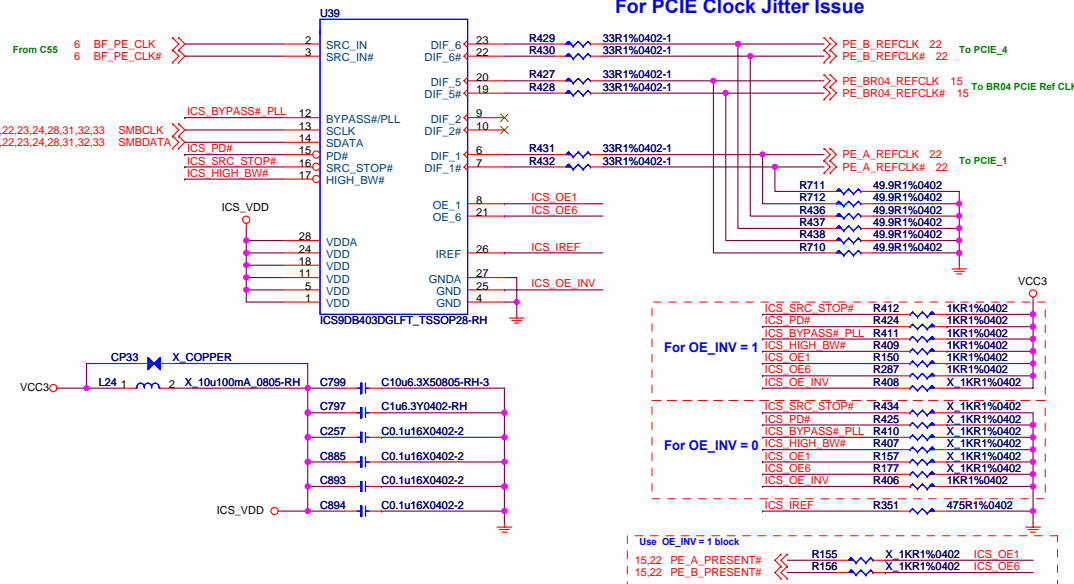
- VCC5 Section:** Features a network of capacitors (C236-C262) connected to a VCC5 supply. It includes a +12V input and a series of capacitors labeled C0.01u25X0402.
- VCC5_SB Section:** Contains capacitors C288 through C299, all specified as X C0.01u25X0402.
- VCC3 Section:** Includes capacitors C884 through C887, all specified as X C0.1u16X0402-2.
- 3VDUAL Section:** Shows a dual supply section with capacitors C890 through C938, primarily specified as X C0.1u16X0402-2.
- CP Section:** Displays a vertical stack of components labeled CP53 through CP44, each marked with X_COPPER.

The diagram uses standard electronic symbols for capacitors, power supplies, and ground connections, with component values and part numbers clearly indicated next to each symbol.

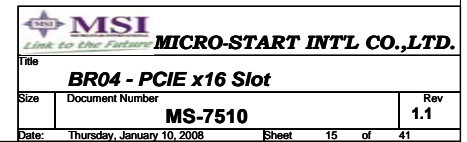
C55 to BR04 PCI-Express Interface



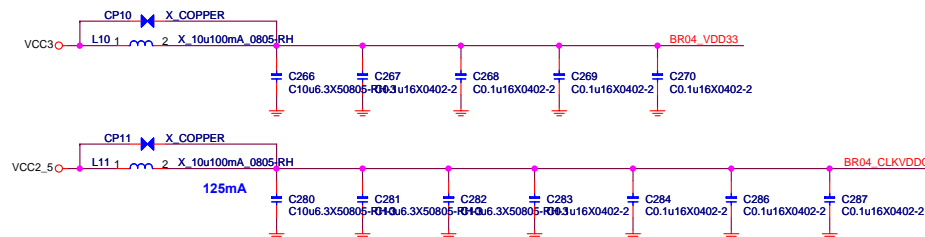
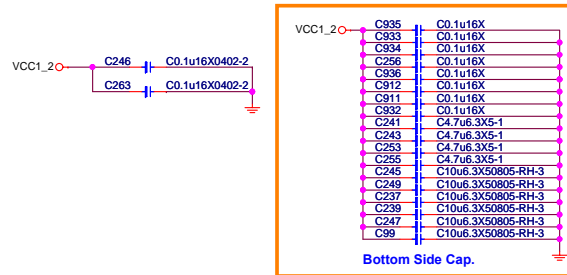
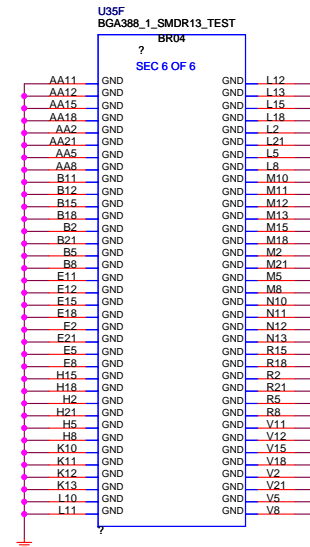
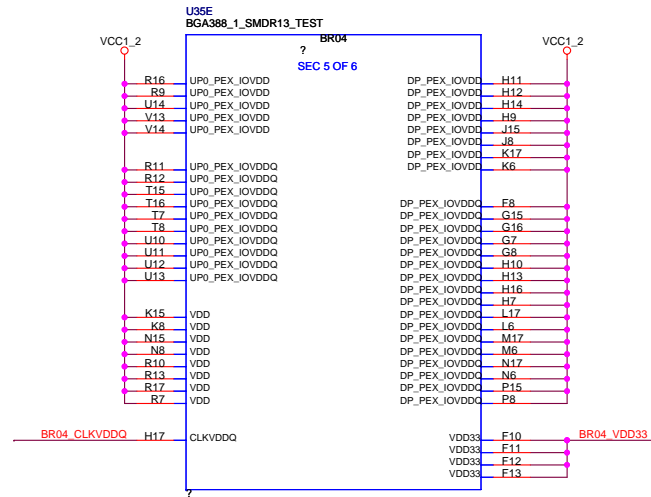
For PCIe Clock Jitter Issue

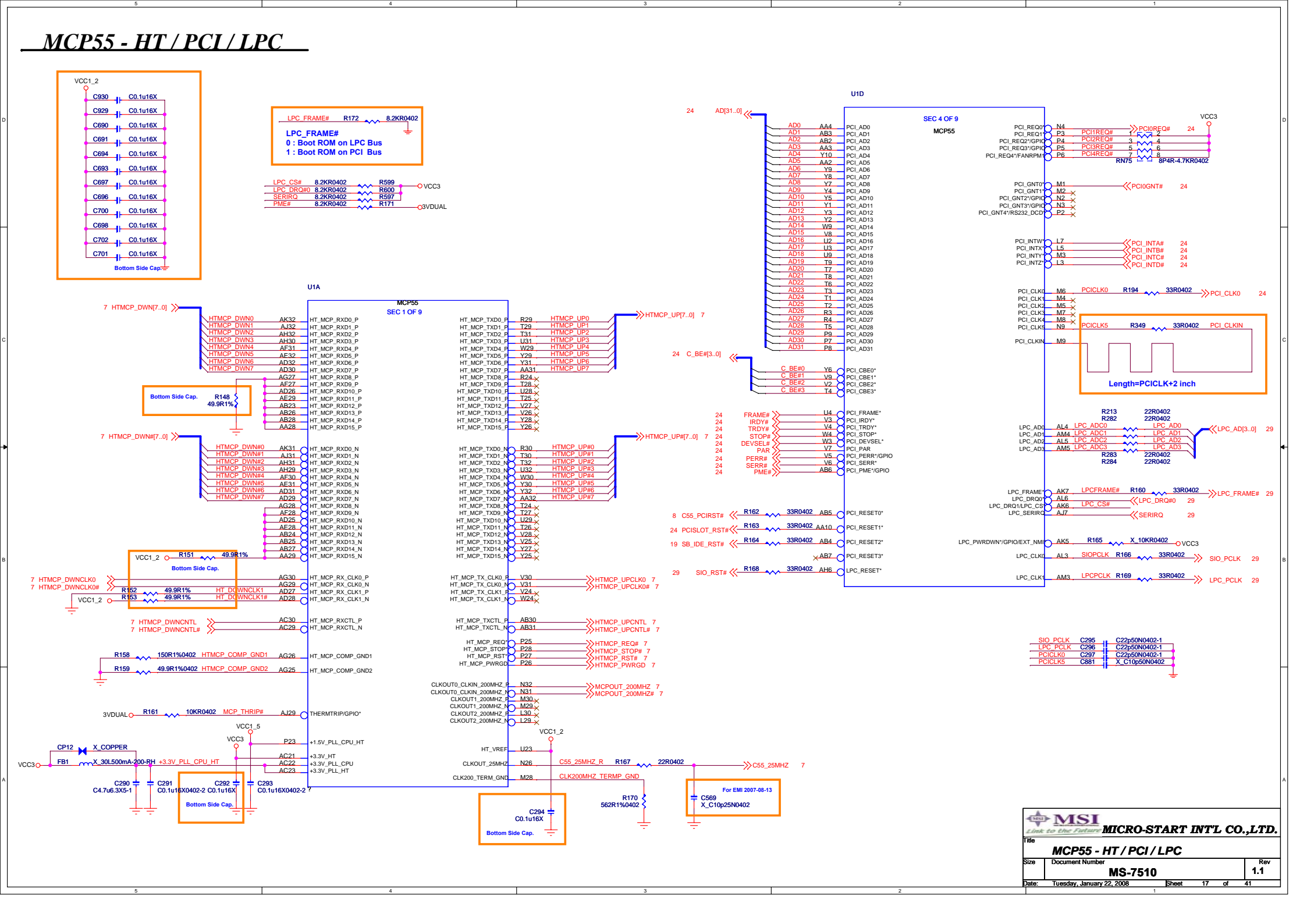


PCB layout diagram for the power plane. The diagram shows a series of decoupling capacitors (C231, C232, C233, C234, C235) connected to a common ground. A note indicates to place the capacitors close to the chipset power pin.



BR04 Power and Gnd Block



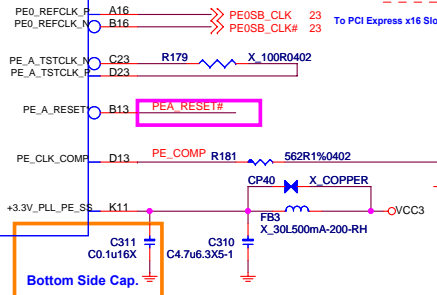
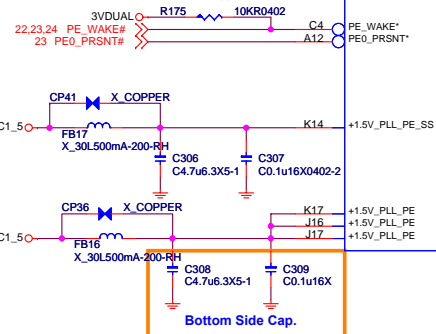
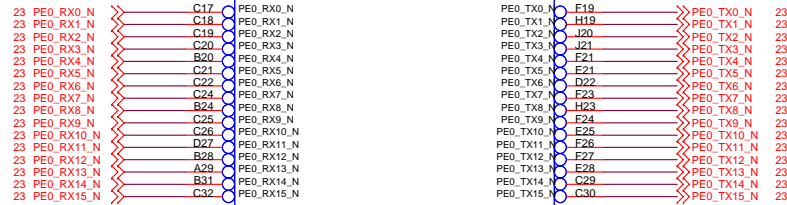
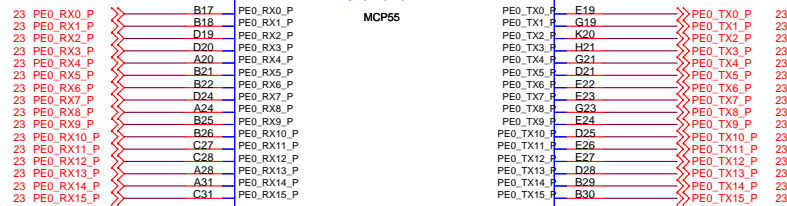
[illegible]

MCP55 - PCI-E

U1B

SEC 2 OF 9

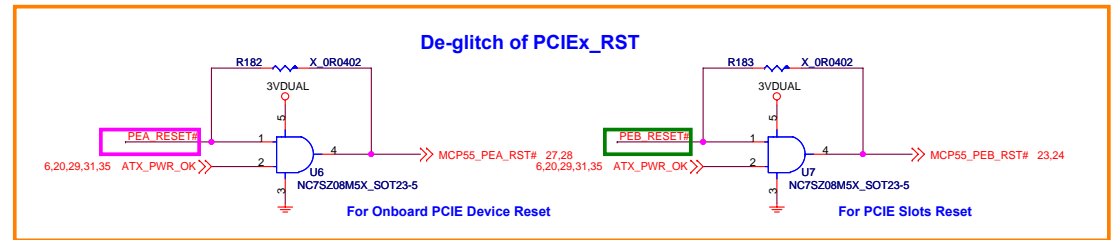
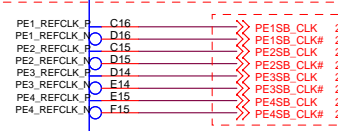
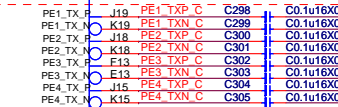
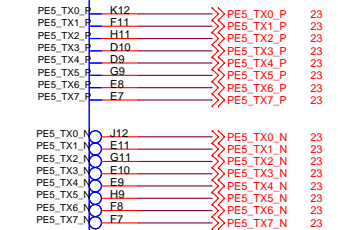
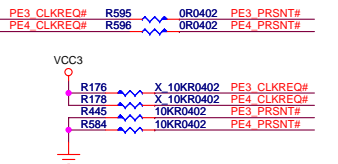
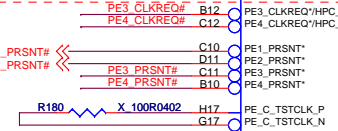
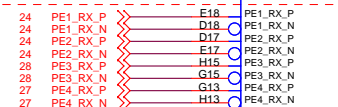
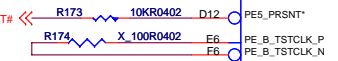
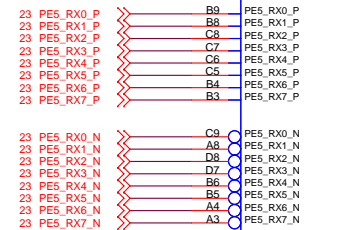
MCP55



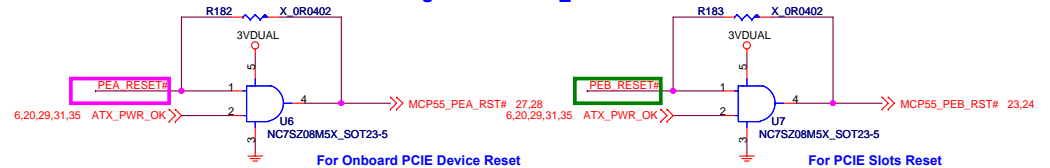
U1C

SEC 3 OF 9

MCP55



De-glitch of PCIe_RST



MCP55 - Audio / USB / GPIO

U1F

SEC 6 OF 9
MCP55

25,26 RGMII_RST#

nvidia suggest
R228 4.7KR0402

For USB power On or Off on First boot on Default : Off

VCC3 R224 10KR0402

TP35 AH18

TP36 AH18

TP37 AH18

TP38 AH18

TP39 AH18

TP40 AH18

TP41 AH18

TP42 AH18

TP43 AH18

TP44 AH18

TP45 AH18

TP46 AH18

TP47 AH18

TP48 AH18

TP49 AH18

TP50 AH18

TP51 AH18

TP52 AH18

TP53 AH18

TP54 AH18

TP55 AH18

TP56 AH18

TP57 AH18

TP58 AH18

TP59 AH18

TP60 AH18

TP61 AH18

TP62 AH18

TP63 AH18

TP64 AH18

TP65 AH18

TP66 AH18

TP67 AH18

TP68 AH18

TP69 AH18

TP70 AH18

TP71 AH18

TP72 AH18

TP73 AH18

TP74 AH18

TP75 AH18

TP76 AH18

TP77 AH18

TP78 AH18

TP79 AH18

TP80 AH18

TP81 AH18

TP82 AH18

TP83 AH18

TP84 AH18

TP85 AH18

TP86 AH18

TP87 AH18

TP88 AH18

TP89 AH18

TP90 AH18

TP91 AH18

TP92 AH18

TP93 AH18

TP94 AH18

TP95 AH18

TP96 AH18

TP97 AH18

TP98 AH18

TP99 AH18

TP100 AH18

TP101 AH18

TP102 AH18

TP103 AH18

TP104 AH18

TP105 AH18

TP106 AH18

TP107 AH18

TP108 AH18

TP109 AH18

TP110 AH18

TP111 AH18

TP112 AH18

TP113 AH18

TP114 AH18

TP115 AH18

TP116 AH18

TP117 AH18

TP118 AH18

TP119 AH18

TP120 AH18

TP121 AH18

TP122 AH18

TP123 AH18

TP124 AH18

TP125 AH18

TP126 AH18

TP127 AH18

TP128 AH18

TP129 AH18

TP130 AH18

TP131 AH18

TP132 AH18

TP133 AH18

TP134 AH18

TP135 AH18

TP136 AH18

TP137 AH18

TP138 AH18

TP139 AH18

TP140 AH18

TP141 AH18

TP142 AH18

TP143 AH18

TP144 AH18

TP145 AH18

TP146 AH18

TP147 AH18

TP148 AH18

TP149 AH18

TP150 AH18

TP151 AH18

TP152 AH18

TP153 AH18

TP154 AH18

TP155 AH18

TP156 AH18

TP157 AH18

TP158 AH18

TP159 AH18

TP160 AH18

TP161 AH18

TP162 AH18

TP163 AH18

TP164 AH18

TP165 AH18

TP166 AH18

TP167 AH18

TP168 AH18

TP169 AH18

TP170 AH18

TP171 AH18

TP172 AH18

TP173 AH18

TP174 AH18

TP175 AH18

TP176 AH18

TP177 AH18

TP178 AH18

TP179 AH18

TP180 AH18

TP181 AH18

TP182 AH18

TP183 AH18

TP184 AH18

TP185 AH18

TP186 AH18

TP187 AH18

TP188 AH18

TP189 AH18

TP190 AH18

TP191 AH18

TP192 AH18

TP193 AH18

TP194 AH18

TP195 AH18

TP196 AH18

TP197 AH18

TP198 AH18

TP199 AH18

TP200 AH18

TP201 AH18

TP202 AH18

TP203 AH18

TP204 AH18

TP205 AH18

TP206 AH18

TP207 AH18

TP208 AH18

TP209 AH18

TP210 AH18

TP211 AH18

TP212 AH18

TP213 AH18

TP214 AH18

TP215 AH18

TP216 AH18

TP217 AH18

TP218 AH18

TP219 AH18

TP220 AH18

TP221 AH18

TP222 AH18

TP223 AH18

TP224 AH18

TP225 AH18

TP226 AH18

TP227 AH18

TP228 AH18

TP229 AH18

TP230 AH18

TP231 AH18

TP232 AH18

TP233 AH18

TP234 AH18

TP235 AH18

TP236 AH18

TP237 AH18

TP238 AH18

TP239 AH18

TP240 AH18

TP241 AH18

TP242 AH18

TP243 AH18

TP244 AH18

TP245 AH18

TP246 AH18

TP247 AH18

TP248 AH18

TP249 AH18

TP250 AH18

TP251 AH18

TP252 AH18

TP253 AH18

TP254 AH18

TP255 AH18

TP256 AH18

TP257 AH18

TP258 AH18

TP259 AH18

TP260 AH18

TP261 AH18

TP262 AH18

TP263 AH18

TP264 AH18

TP265 AH18

TP266 AH18

TP267 AH18

TP268 AH18

TP269 AH18

TP270 AH18

TP271 AH18

TP272 AH18

TP273 AH18

TP274 AH18

TP275 AH18

TP276 AH18

TP277 AH18

TP278 AH18

TP279 AH18

TP280 AH18

TP281 AH18

TP282 AH18

TP283 AH18

TP284 AH18

TP285 AH18

TP286 AH18

TP287 AH18

TP288 AH18

TP289 AH18

TP290 AH18

TP291 AH18

TP292 AH18

TP293 AH18

TP294 AH18

TP295 AH18

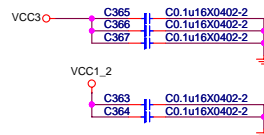
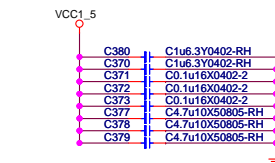
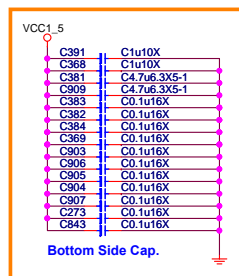
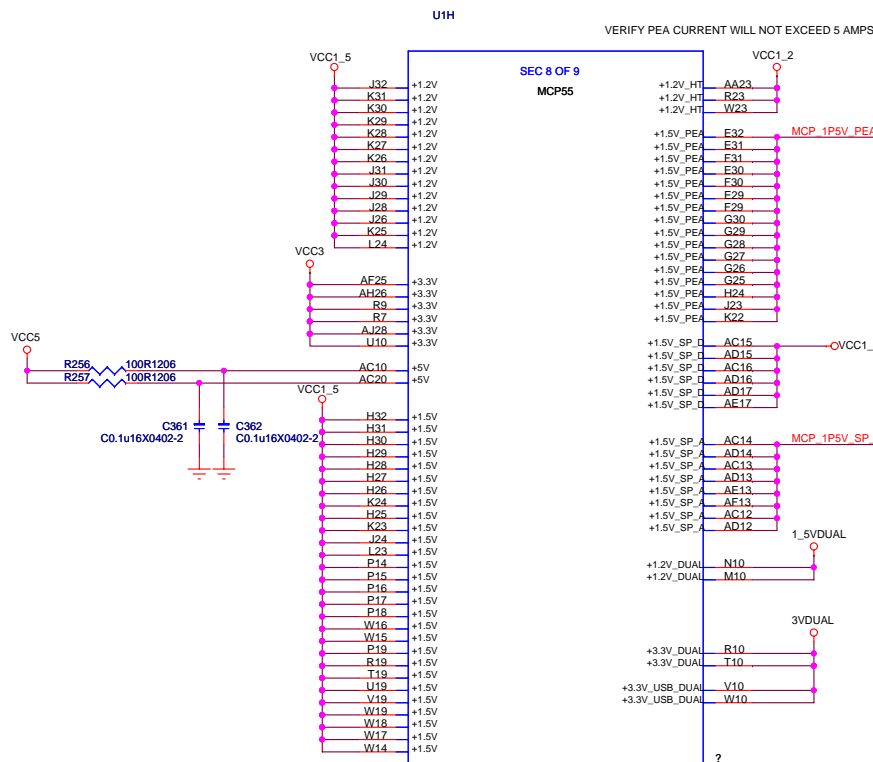
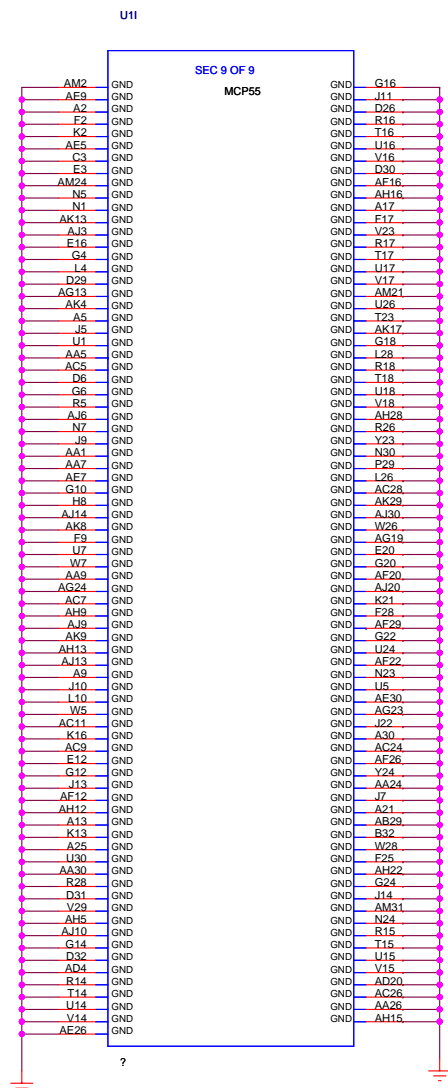
TP296 AH18

TP297 AH18

TP298 AH18

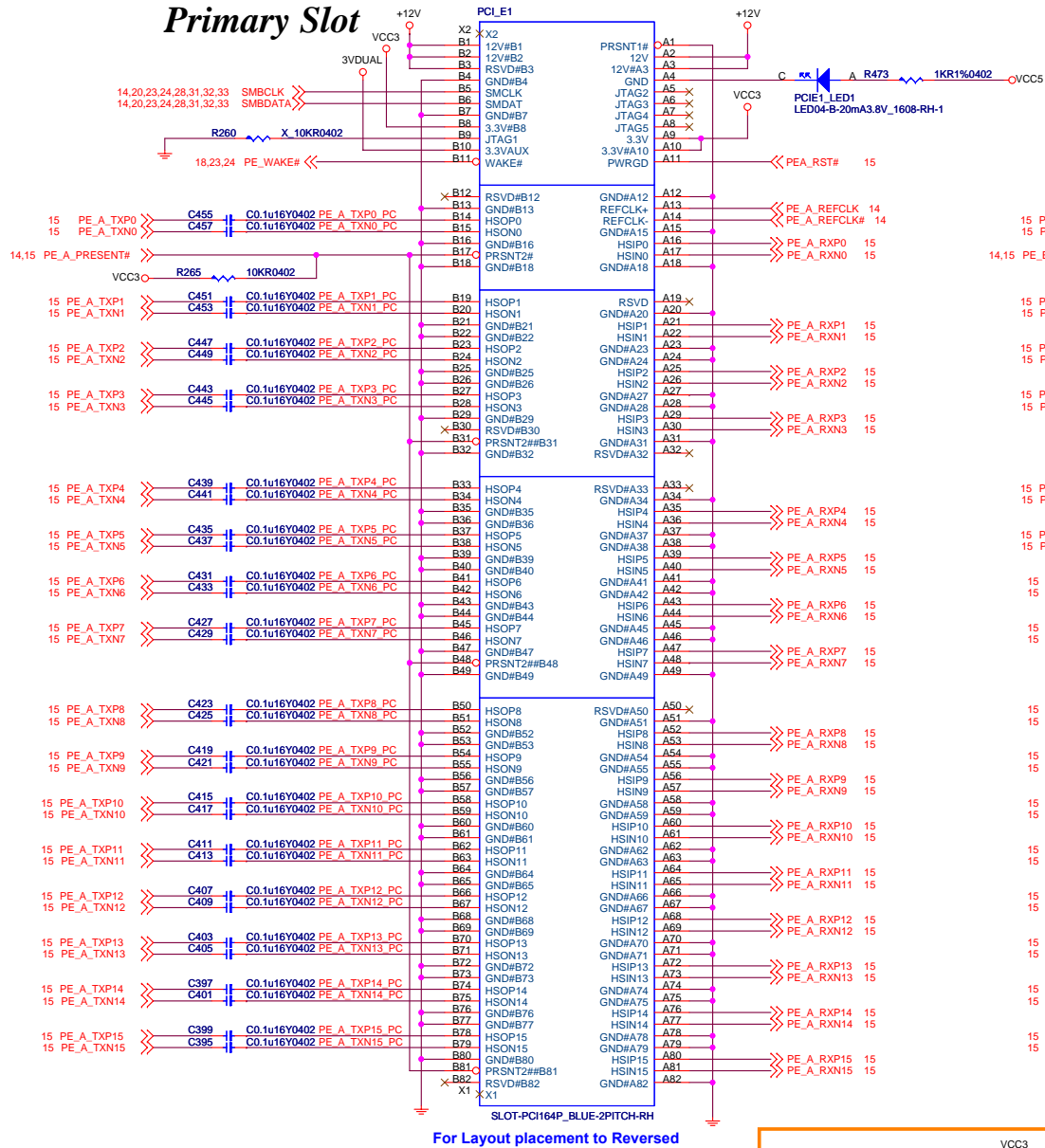
TP299 AH18

MCP55 - Power & Gnd

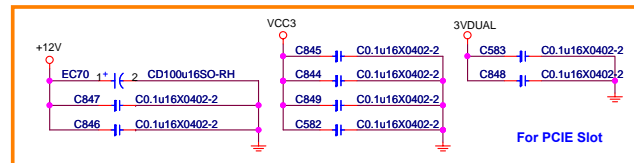
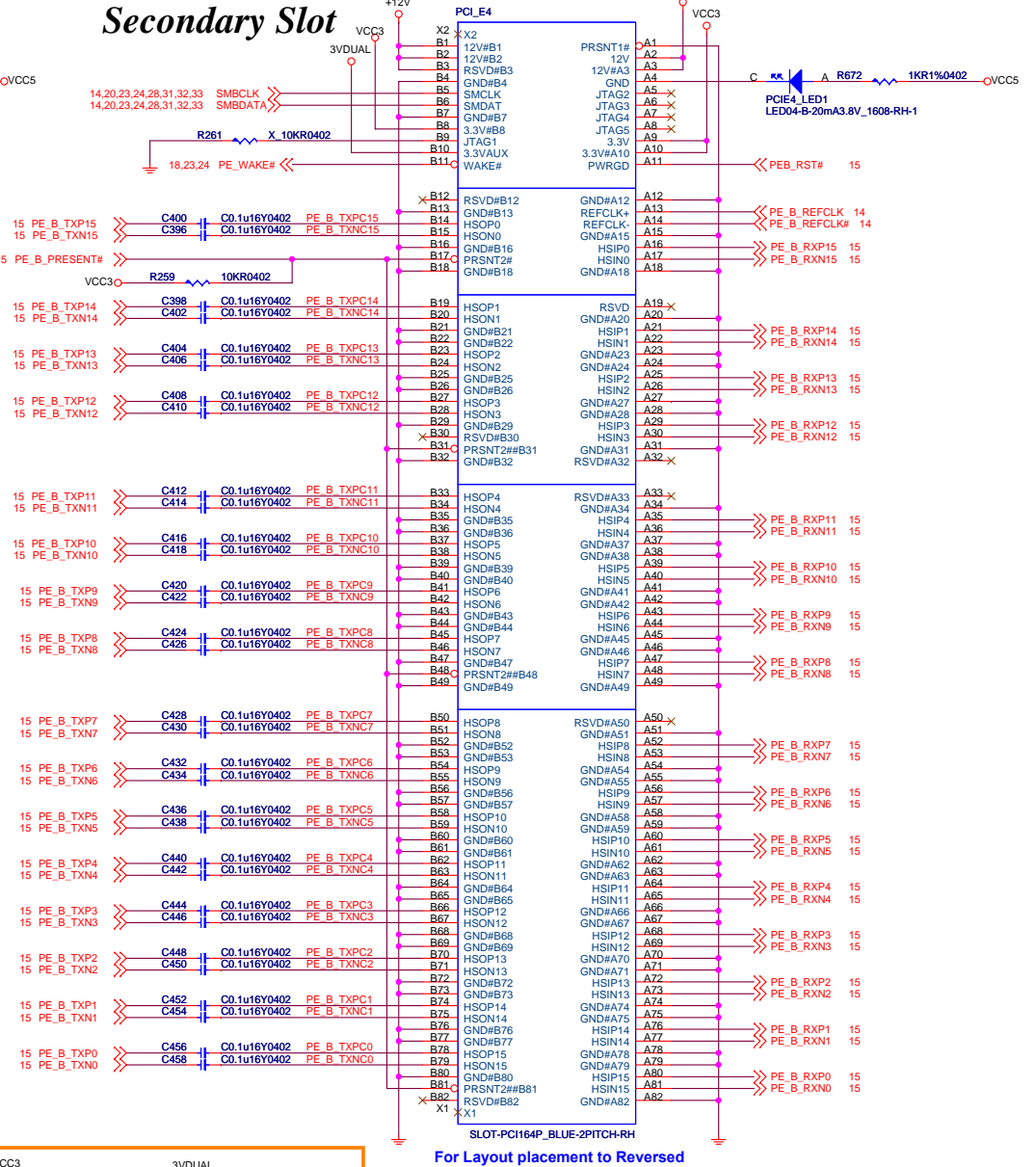


PCI-Express x16 Primary and Secondary Slot

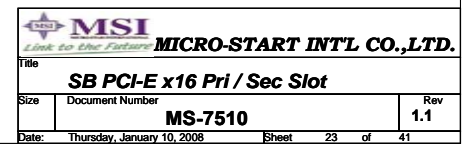
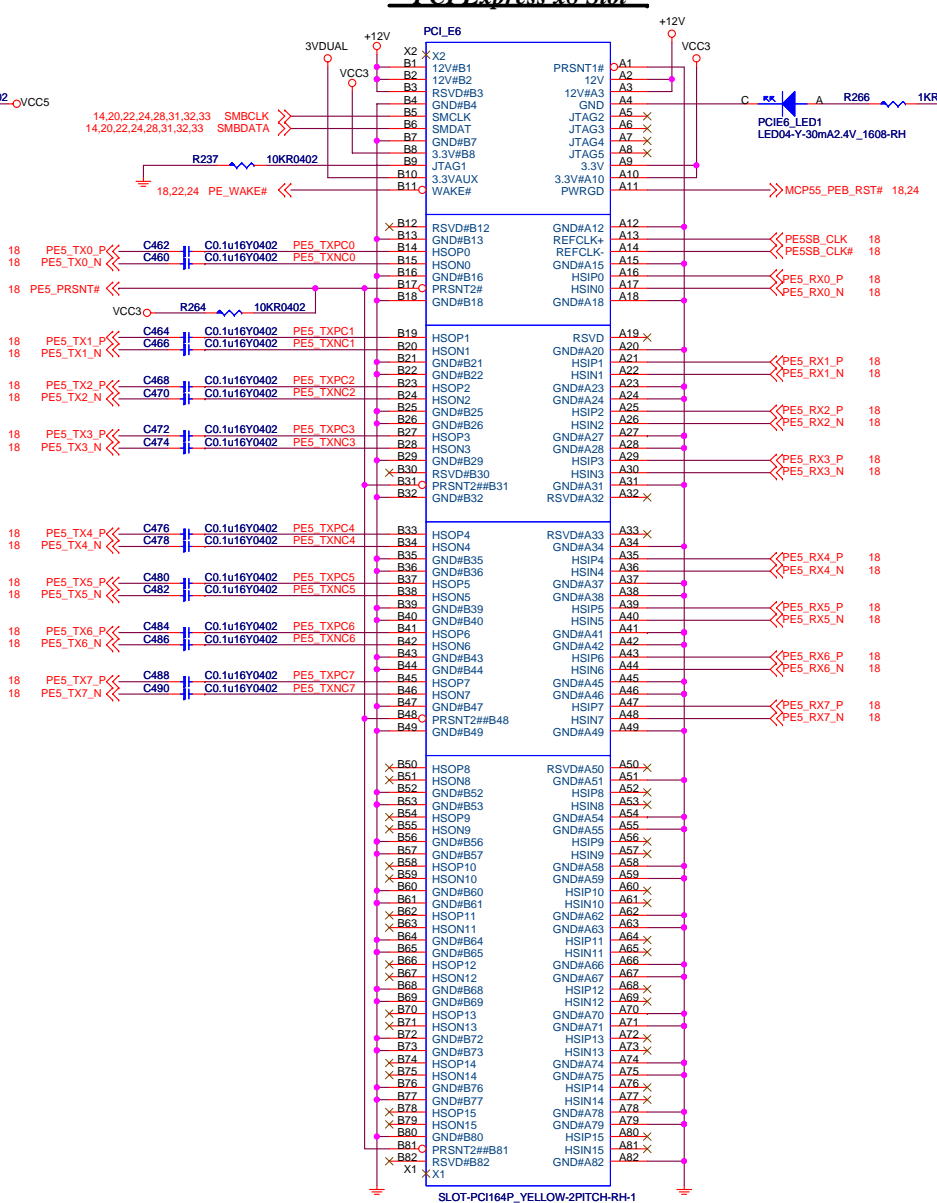
Primary Slot



Secondary Slot

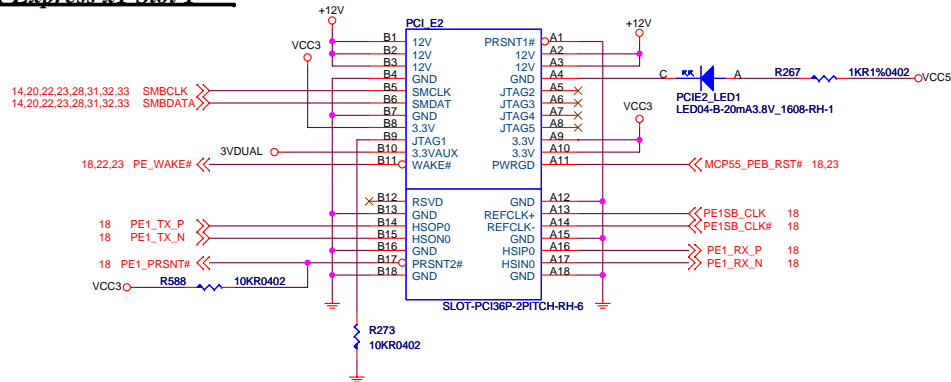


PCI Express x8 Slot

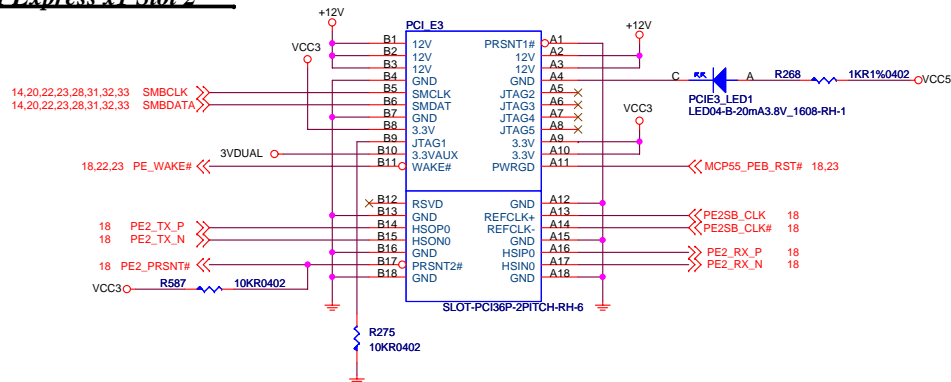


SB PCI-Express x1 Slots and PCI Slot

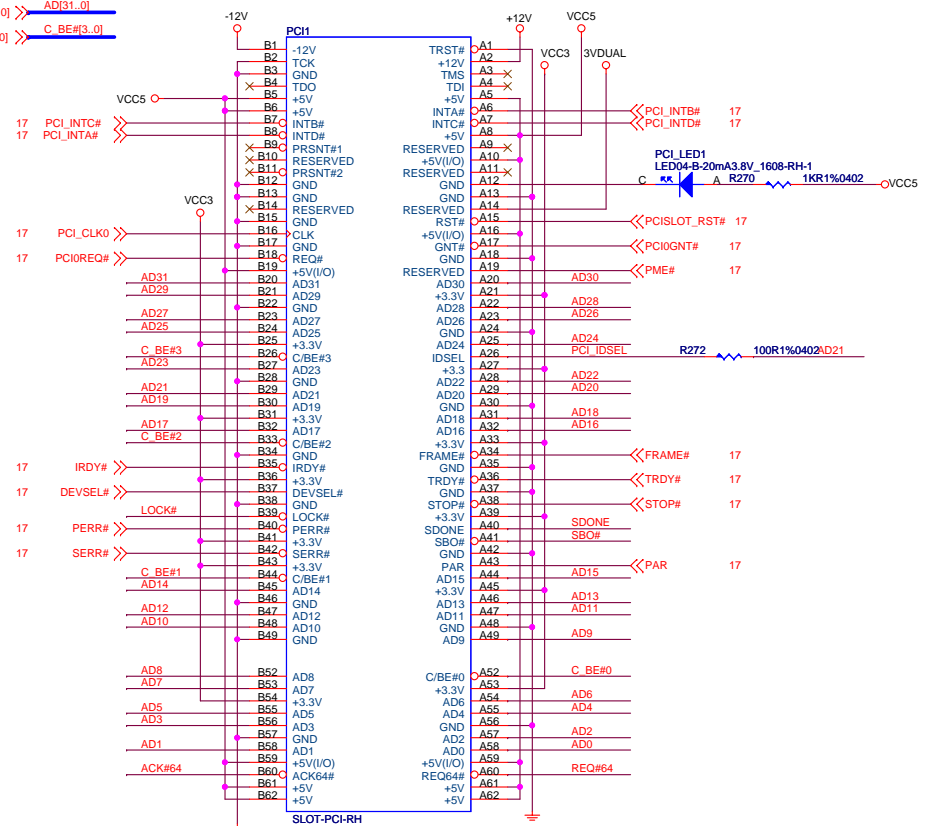
PCI Express x1 Slot 1



PCI Express x1 Slot 2

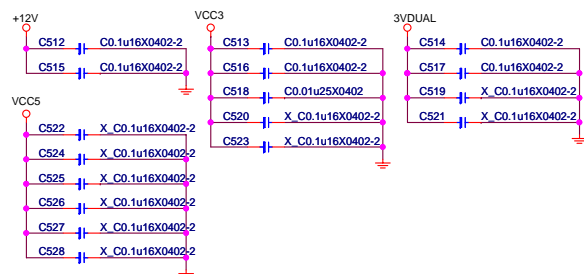


PCI Slot 1 (PCIVER: 2.2 Comply)

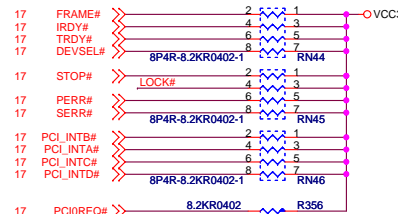


IDSEL = AD21
MASTER = PCI0REQ#
PCI0GNT*

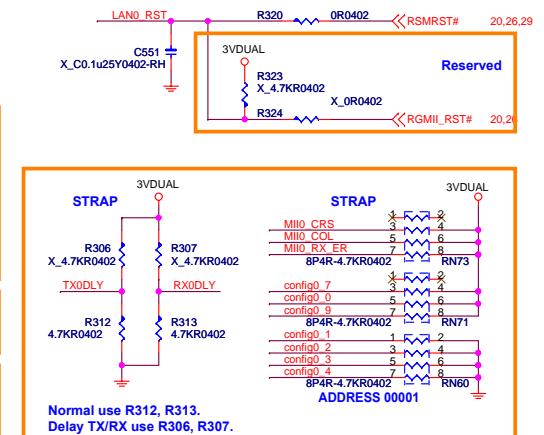
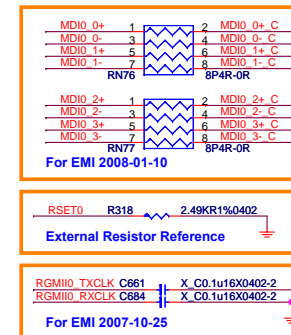
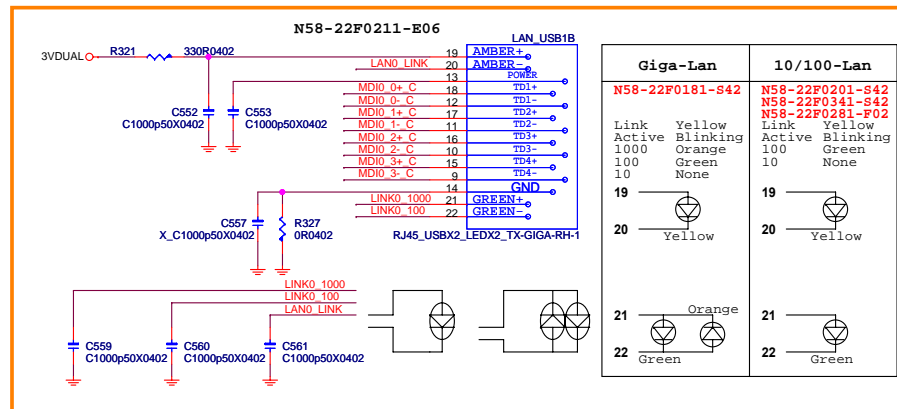
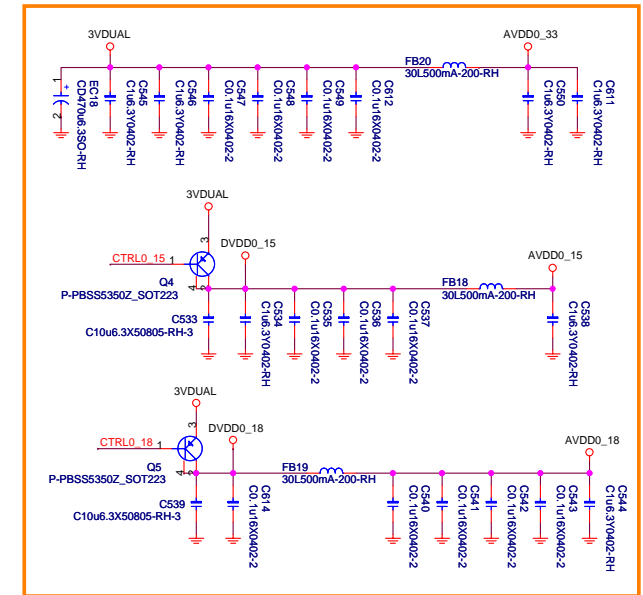
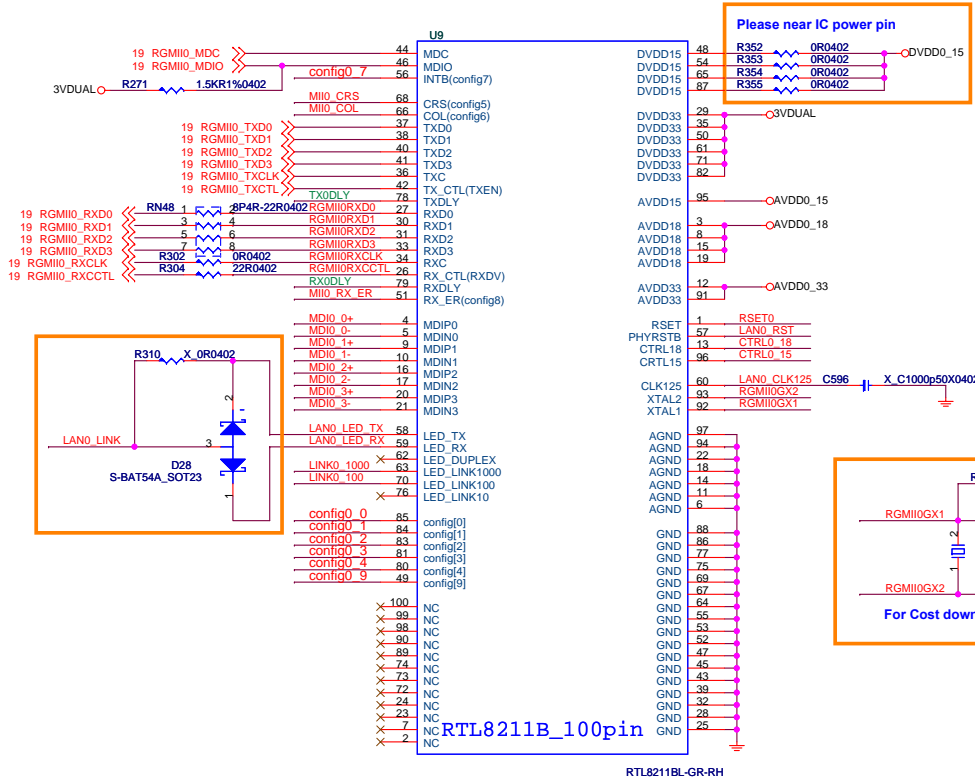
PCISlot Decoupling Capacitors



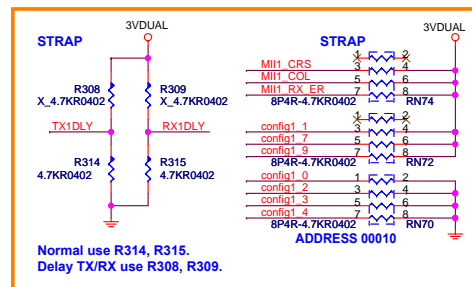
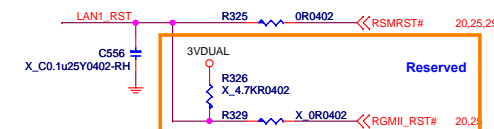
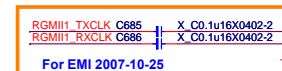
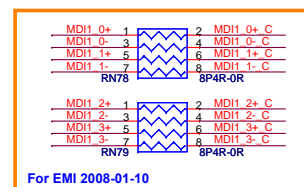
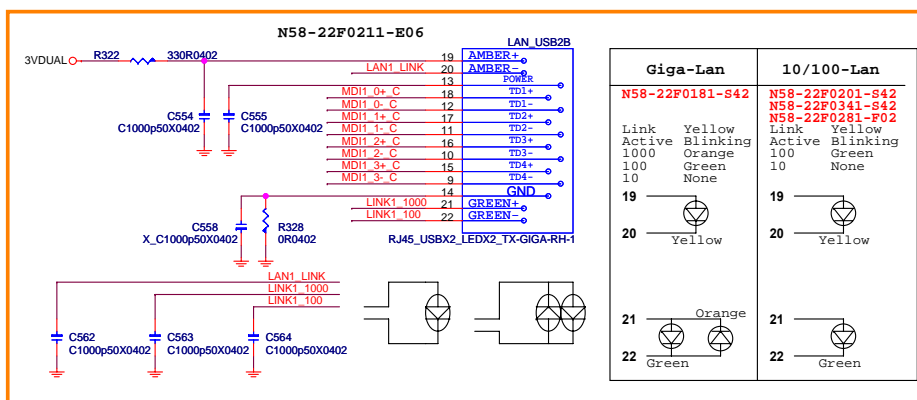
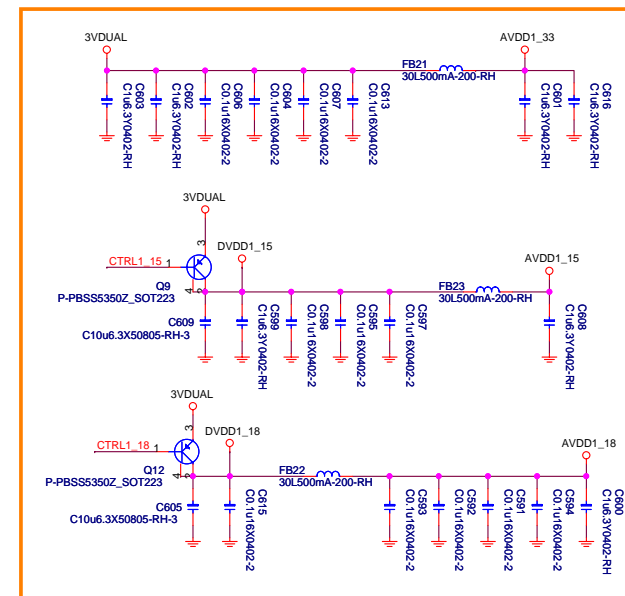
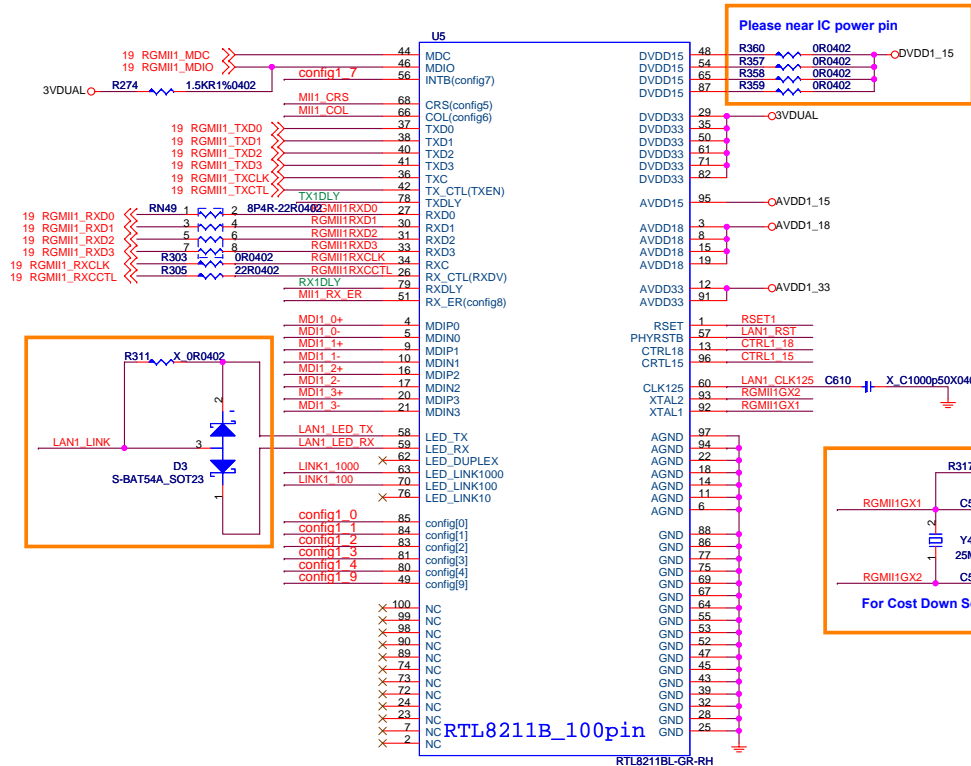
PCI Pull Up / Down Resistors



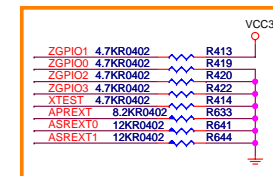
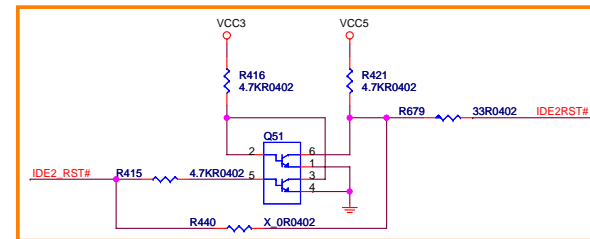
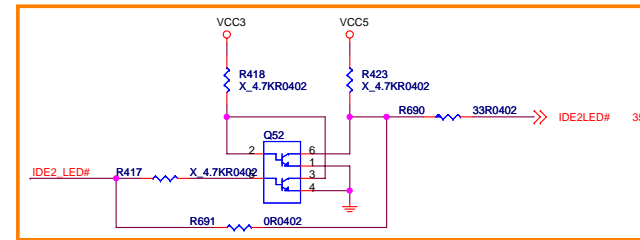
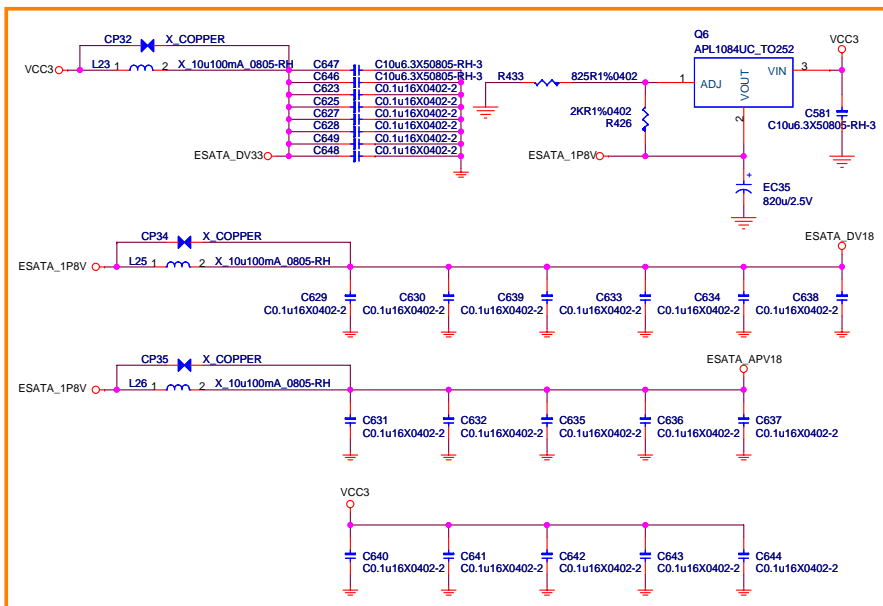
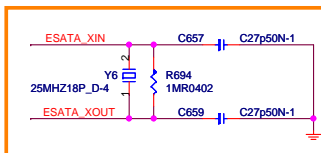
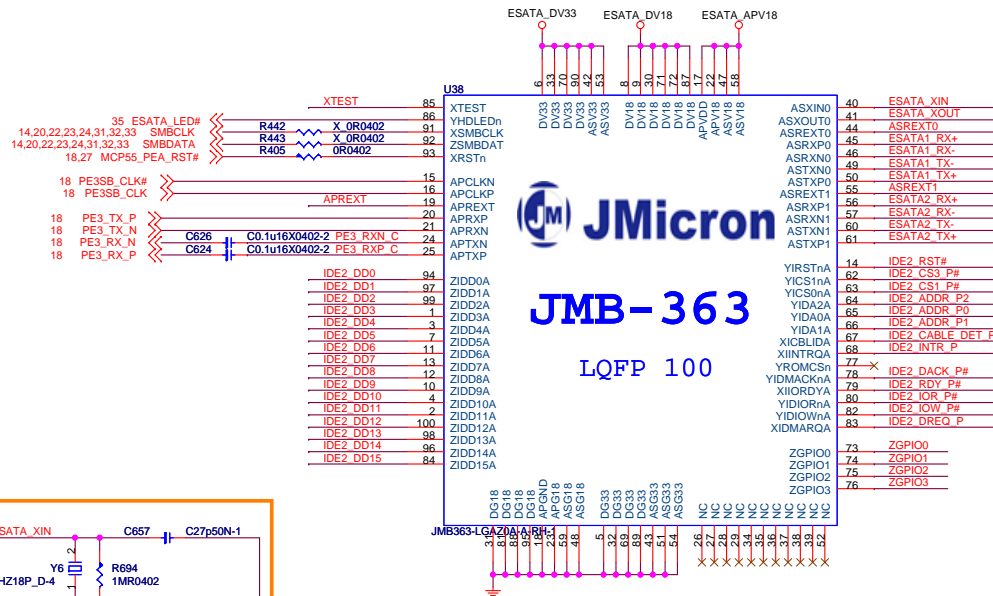
RealTek RTL8211B RGMII Gigabit PHY (Lan 0)



RealTek RTL8211B RGMII Gigabit PHY (Lan 1)



JMicron JMB363 eSATA Controller

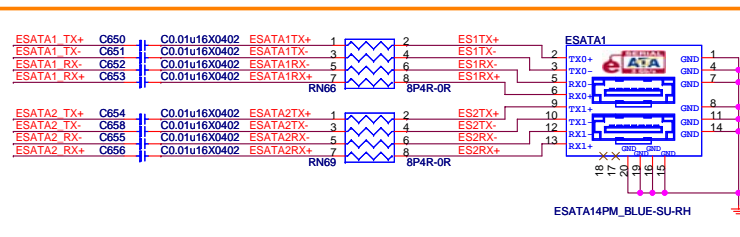
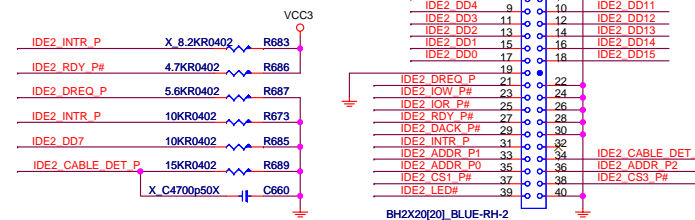


SATA II Port 0 External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground ASG18 (pin#48).

SATA II Port 0 External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground ASG18 (pin#59).

PCI Express External Reference Resistor.
An external 12KΩ±1% resistor should be connected and bypass to the ground APG18 (pin#18).

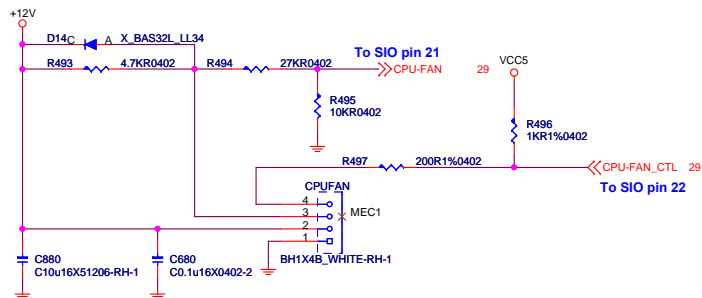
PATA 66/100/133 Connector



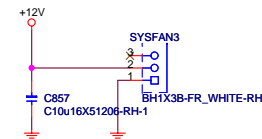
JMB363 GPIO0
It uses to control function# available on JMB363.
0: single function ; 1: multi-function
JMB363 GPIO1
It uses to control clock source of SATA II port 0.
0: from internal clock source from PCI Express clock source
1: from ASXIN0 & ASXOUT0
JMB363 GPIO2
It uses to control interface to access internal debug registers.
0: SMBus I/F ; 1: Reserved for debugging.
JMB363 GPIO3
Reserved for debugging.
JMB363 Test Mode Enable
High-active signal to enable testing and debug modes of JMB363.

Fan Controller

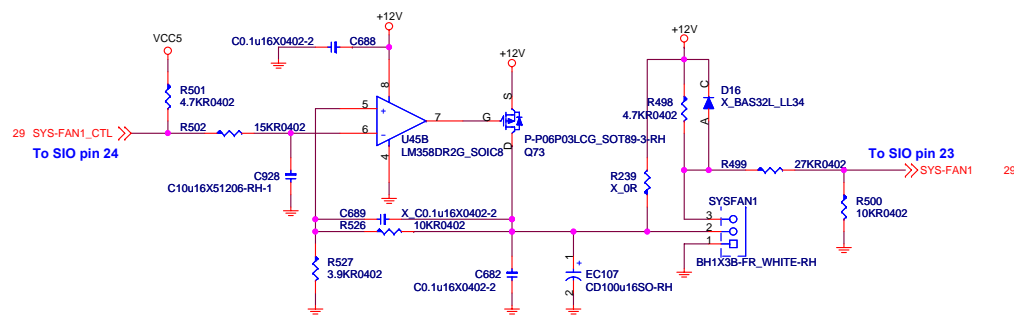
CPU Fan



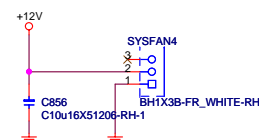
System Fan 3



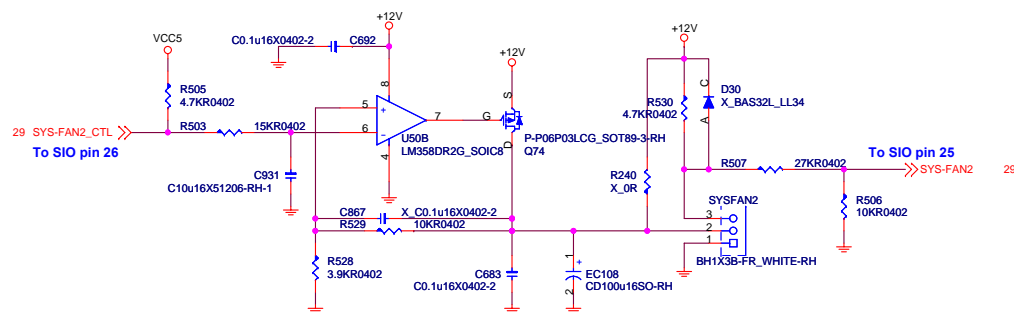
System Fan 1



System Fan 4

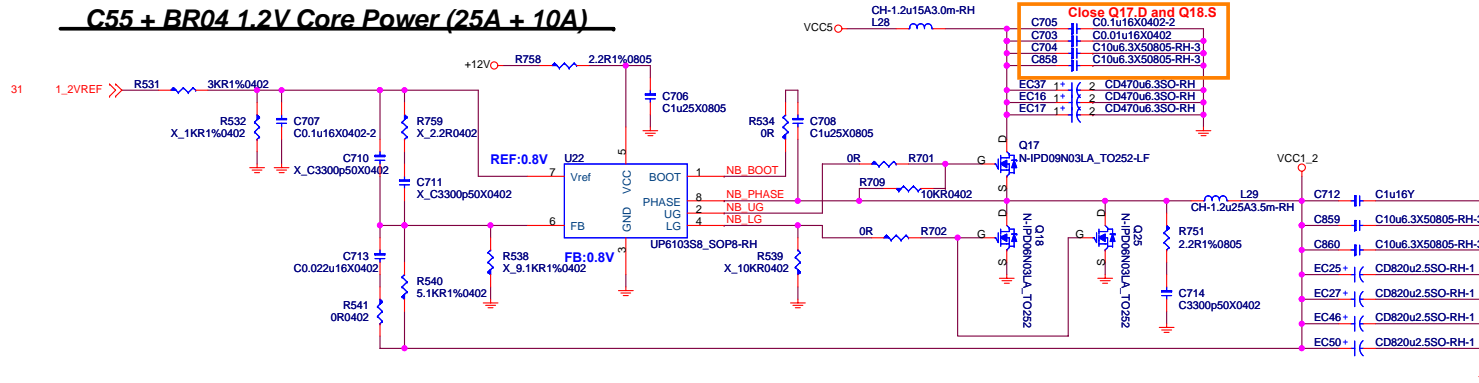


System Fan 2

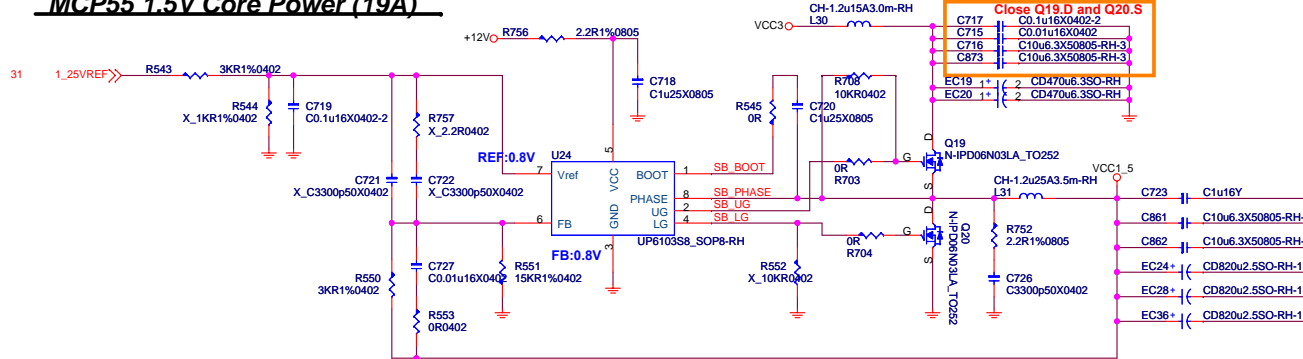


uPI Power Regulator

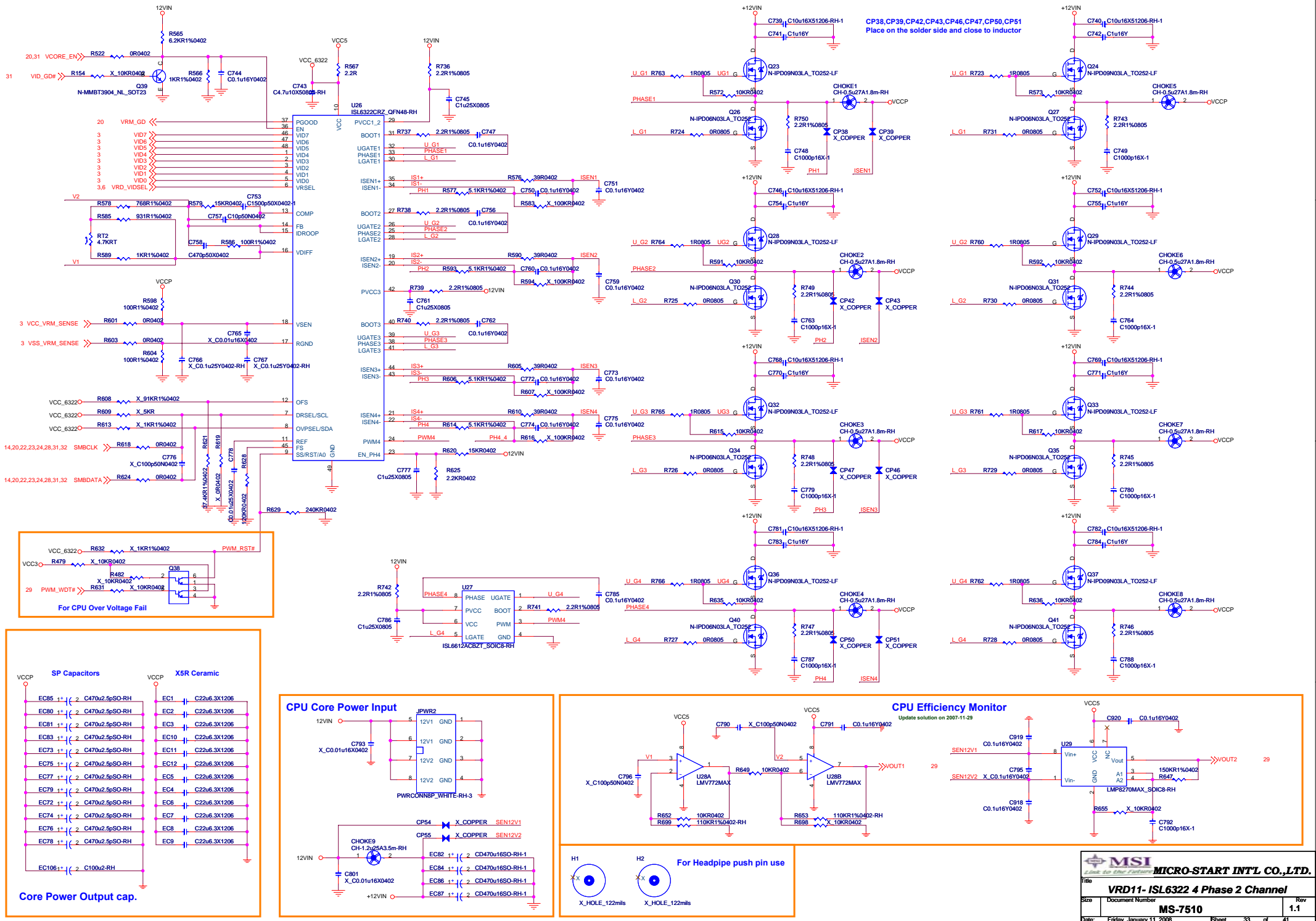
C55 + BR04 1.2V Core Power (25A + 10A)



MCP55 1.5V Core Power (19A)

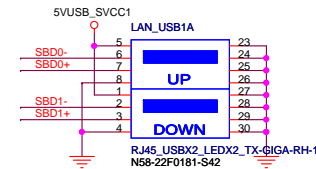
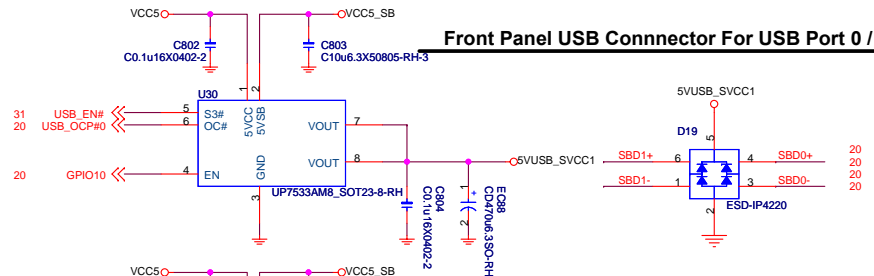


Voltage Regular Module (VRD11)

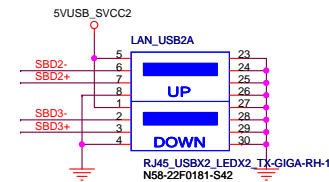
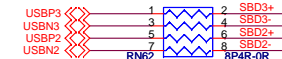
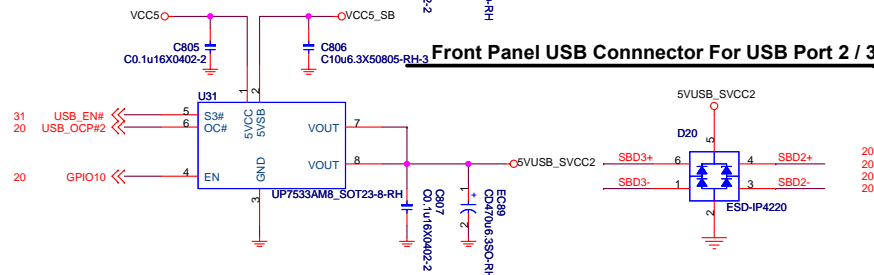


Front Panel and Real I/O USB Connector

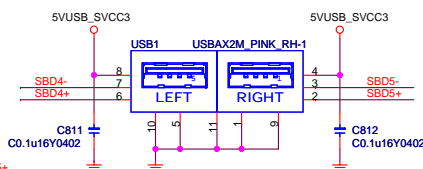
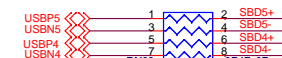
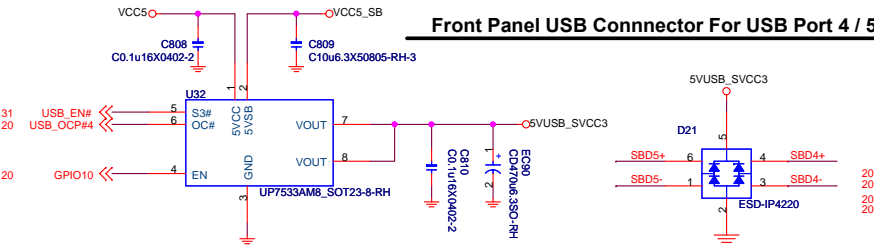
Front Panel USB Connector For USB Port 0 / 1



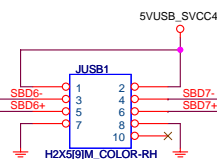
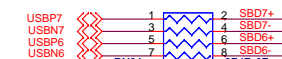
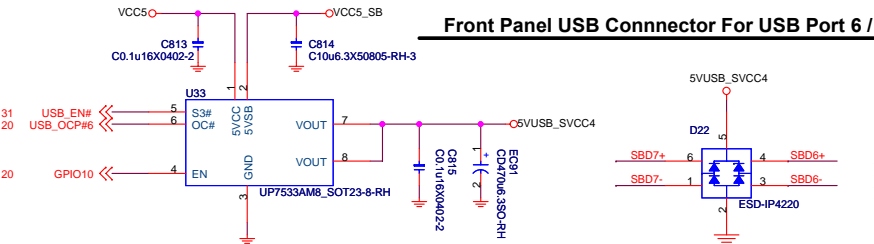
Front Panel USB Connector For USB Port 2 / 3



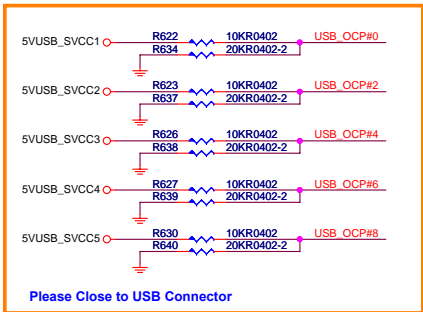
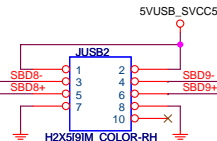
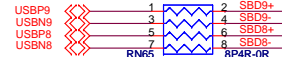
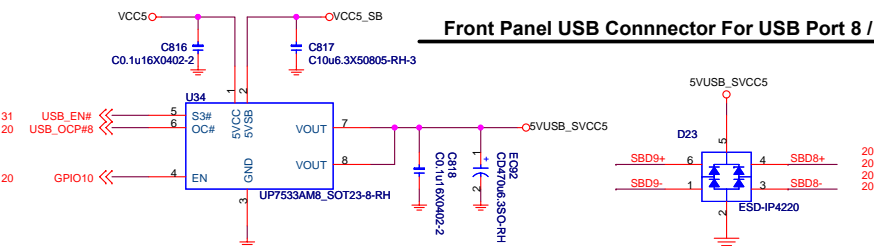
Front Panel USB Connector For USB Port 4 / 5

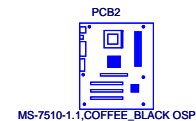
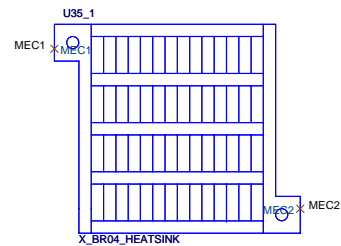
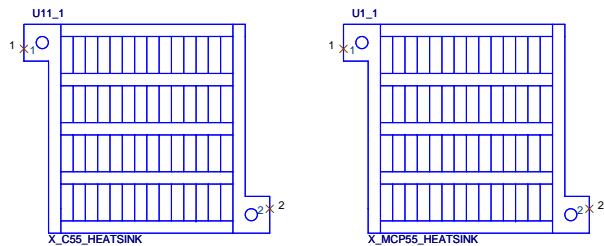


Front Panel USB Connector For USB Port 6 / 7

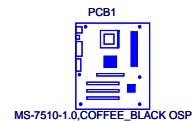


Front Panel USB Connector For USB Port 8 / 9

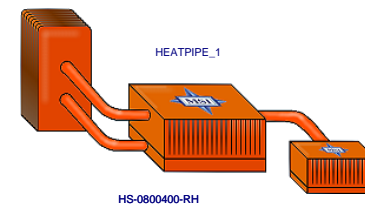




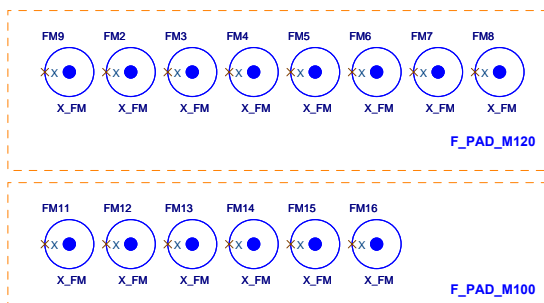
PD0-0751011-E48 (競華)
PD0-0751011-Y43 (育富)



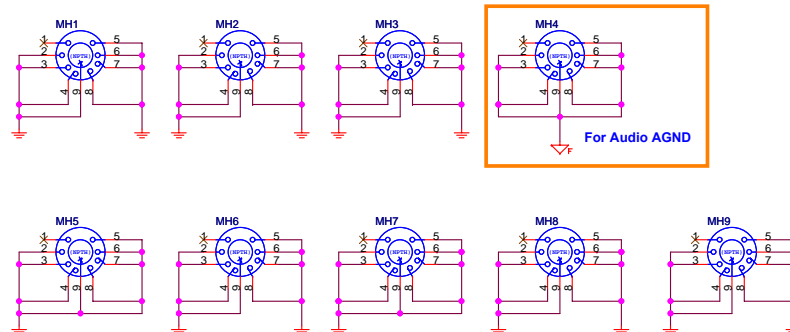
PD0-0751010-D05 (昆頻)
PD0-0751010-Y43 (育富)



Optics Orientation Holes

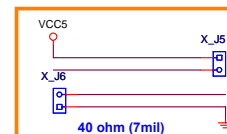
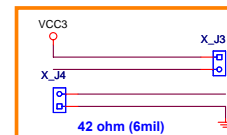
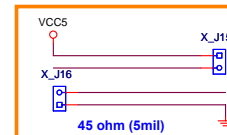
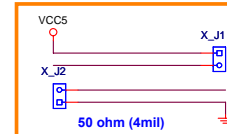


PCB Mounting Holes

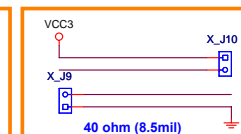
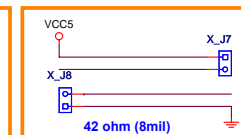
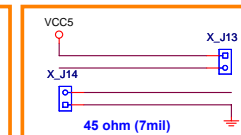
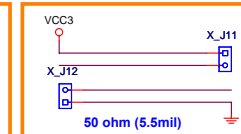


Simulation

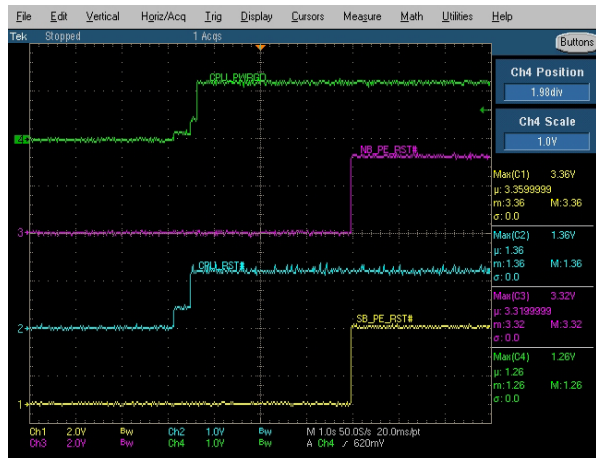
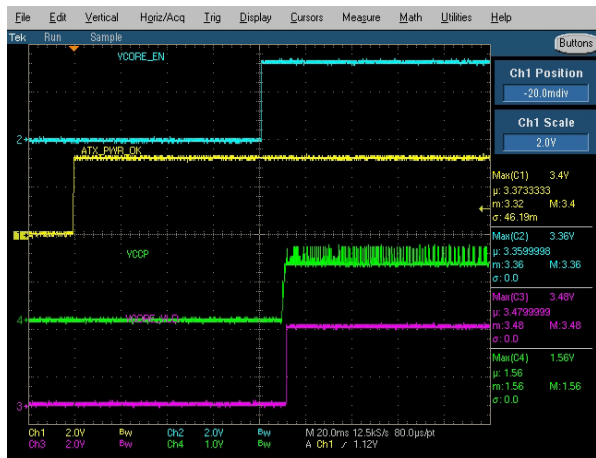
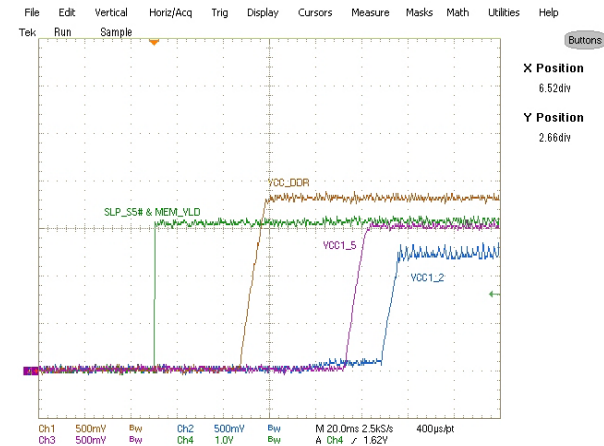
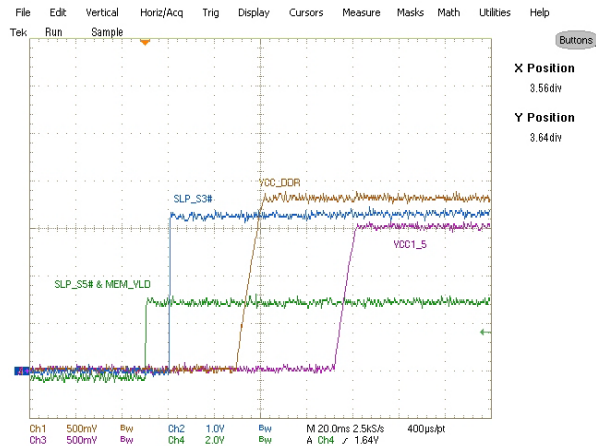
Top and Bottom layer



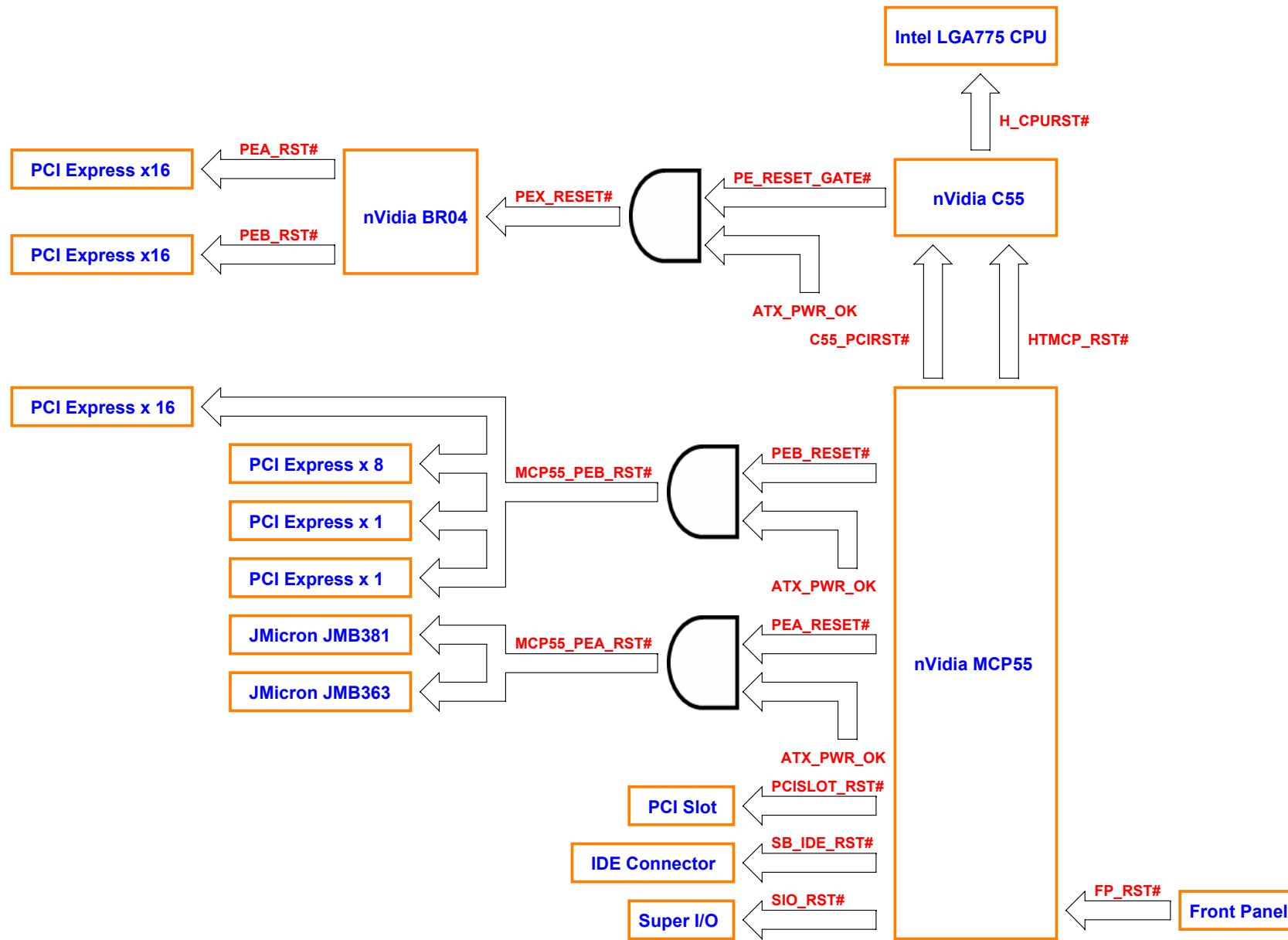
INT1 and INT2 layer



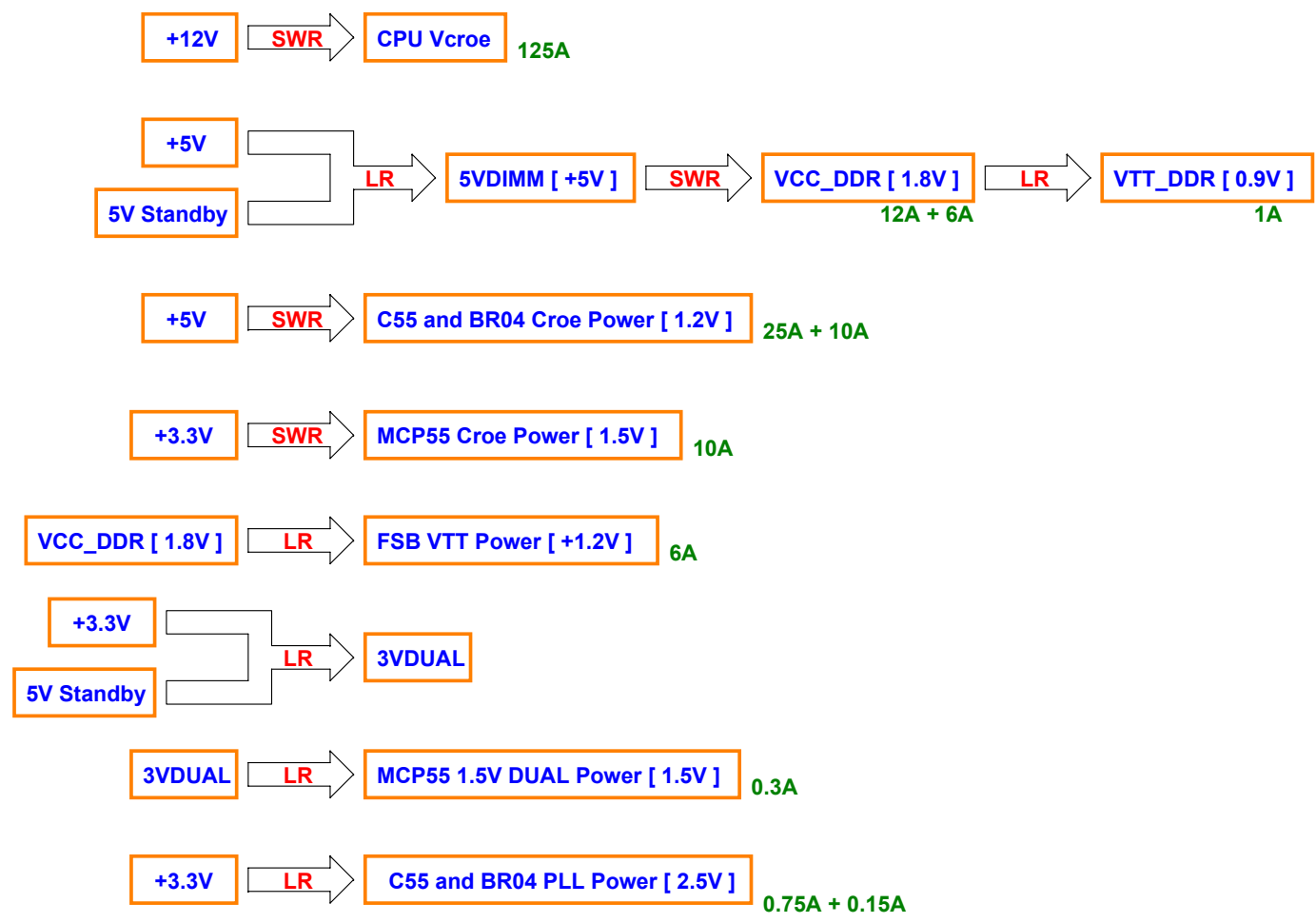
Power On/Off Sequence



System Reset Map



Syatem Power Map



Configuration & GPIO

PCI Configuration

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK	PCI Reset
PCI slot 1	PIRQ#A	PCIOREQ# PCIOGNT#	AD21	PCI_CLK0	PCISLOT_RST#

DDRII DIMM Configuration

DIMM1	DIMM2	DIMM3	DIMM4
A0 1010000B	A4 1010010B	A2 1010001B	A6 1010011B
0A	0B	1A	1B

SMBus Distribution

SMBus	Power	Load
SMBDATA SMBCLK	VCC3	MCP55 , JM363 , PWM , Super I/O , uPI Power IC PCI Express x16 Slot * 3 , PCI Express x 8 Slot * 1 , PCI Express x 1 Slot * 1 , PCI Slot
SMB_MEM_DATA SMB_MEM_CLK	VCC3_SB	MCP55

System Reset Signal

Signal	Device
PE_RESET#	BR04
H_CPURST#	CPU
HTMCP_RST#	C55
PE_A_RESET#	BR04 PCI Express x 16 Primary Slot
PE_B_RESET#	BR04 PCI Express x 16 Secondary Slot
PEA_RESET#	JMicron JMB363 eSATA Controller JMicron JMB381 IEEE 1394a Host Controller
PEB_RESET#	MCP55 PCI Express x 16 Slot MCP55 PCI Express x 8 Slot MCP55 PCI Express x 1 Slot
PCISLOT_RST#	MCP55 PCI Slot
C55_PCIRST#	C55
SB_IDE_RST#	Master IDE Connector
SIO_RST#	Super I/O

SuperI/O GPIO Function

Pin Name	Function Description
GP4	CPU_GTL_REF Select
GP5	Reset PWM
SLOT0CC#	Detect CPU remove or not
COPEN#	Detect Case Open or not
GP23	BOM Select

MCP55 GPIO Function

Pin Name	Function Description
GP10	For USB connector power default on / off

Device Clock Signal

Signal	Device
CK_H_CPU# CK_H_CPU	C55 to CPU
HTMCP_DWNCLK0 HTMCP_DWNCLK0#	C55 to MCP55
HTMCP_UPCLK0 HTMCP_UPCLK0#	MCP55 to C55
PE_BR04_CLK PE_BR04_CLK#	C55 to BR04
BF_PE_CLK BF_PE_CLK#	C55 to Clock Buffer
PE_BR04_REFCLK PE_BR04_REFCLK#	Clock Buffer to BR04
PE_A_REFCLK PE_A_REFCLK#	Clock buffer to Express x 16 Primary Slot
PE_B_REFCLK PE_B_REFCLK#	Clock Buffer to Express x 16 Secondary Slot
MCPOUT_200MHZ MCPOUT_200MHZ#	MCP55 to C55
C55_25MHZ	MCP55 to C55
PE0SB_CLK PE0SB_CLK#	MCP55 to Express x 16 Slot
PE5SB_CLK PE5SB_CLK#	MCP55 to Express x 8 Slot
PE1SB_CLK PE1SB_CLK# PE2SB_CLK PE2SB_CLK#	MCP55 to PCI Express x 1 Slot
PE3SB_CLK PE3SB_CLK#	MCP55 to JMicron JMB363 eSATA Controller
PE4SB_CLK PE4SB_CLK#	MCP55 to JMicron JMB381 IEEE1394a Controller
PCI_CLK0	MCP55 to PCI Slot
SIO_PCLK	MCP55 to FinTek 71883FG Super I/O
LPC_PCLK	MCP55 to JTPM Pin Header

2007-07-25
Crate First Version Schematic

2007-08-08
7510-0A Net-in

2007-08-22
Update project Spec.
From PDC42819 change to JMB363

2007-09-07
Update nVidia PCI Express clock jitter issue solution

2007-09-12
Gerber Out

2007-09-25
Assembly

2007-10-01
HW gat sample board

2007-10-16
7510-0B Net-in
Update circuit
1. Change ACPI solution from MS12 to uPI
2. Modify PCB height and layer stack-up
3. Add SB Side SPI Interface Circuit

2007-10-30
7510-0B Gerber Out

2007-11-11
Assembly

2007-11-27
7510-1.0 Net-in
Update circuit
1. Change SYSFAN1 and SYSFAN2 control circuit solution from PWM Mode to Liner Mode
2. Remove SB Side SPI Interface Circuit
3. Remove CPU PLL liner regular power circuit
4. Remove 1.2V HT liner regular power circuit
5. Modify 3VDUAL liner regular power circuit
6. Add SIO GPIO control for BOM selcet
7. Modify thermal sensor circuit
8. Add nVidia work around of Intel Yourfield CPU
9. Remove debug LED dispaly port circuit

2007-12-07
7510-0B Gerber Out

2007-12-19
Assembly

2007-12-24
HW gat sample board

2008-01-10
7510-1.1 Net-in
Update circuit
1. Modify SYSFAN1 and SYSFAN2 control circuit for can't control issue
2. Remove HDA circuit of EMI request
3. Modify PHY chipset power solution
4. Add EMI solution of 7510-1.0 PCB EMI issue